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MS-7920

Intel -SharkBay plamform Z97

MIN ITX

Ver:10(17x17)

CPU:

System Chipset:

Haswell-R LGA1150

Lynx Point Z97

Onboard Chip:

HD Audio Codec:ALC1150 WiFi / BT: Rear IO Pinheader

LAN-Atheros E2205-B

SIO:Nuvoton 6792

Flash ROM: SPI 64 MB

Main Memory:

DDRIII (1066/1333/1600MHz) * 2 (Dual Channel)

ACPI:

PWM:

UPI

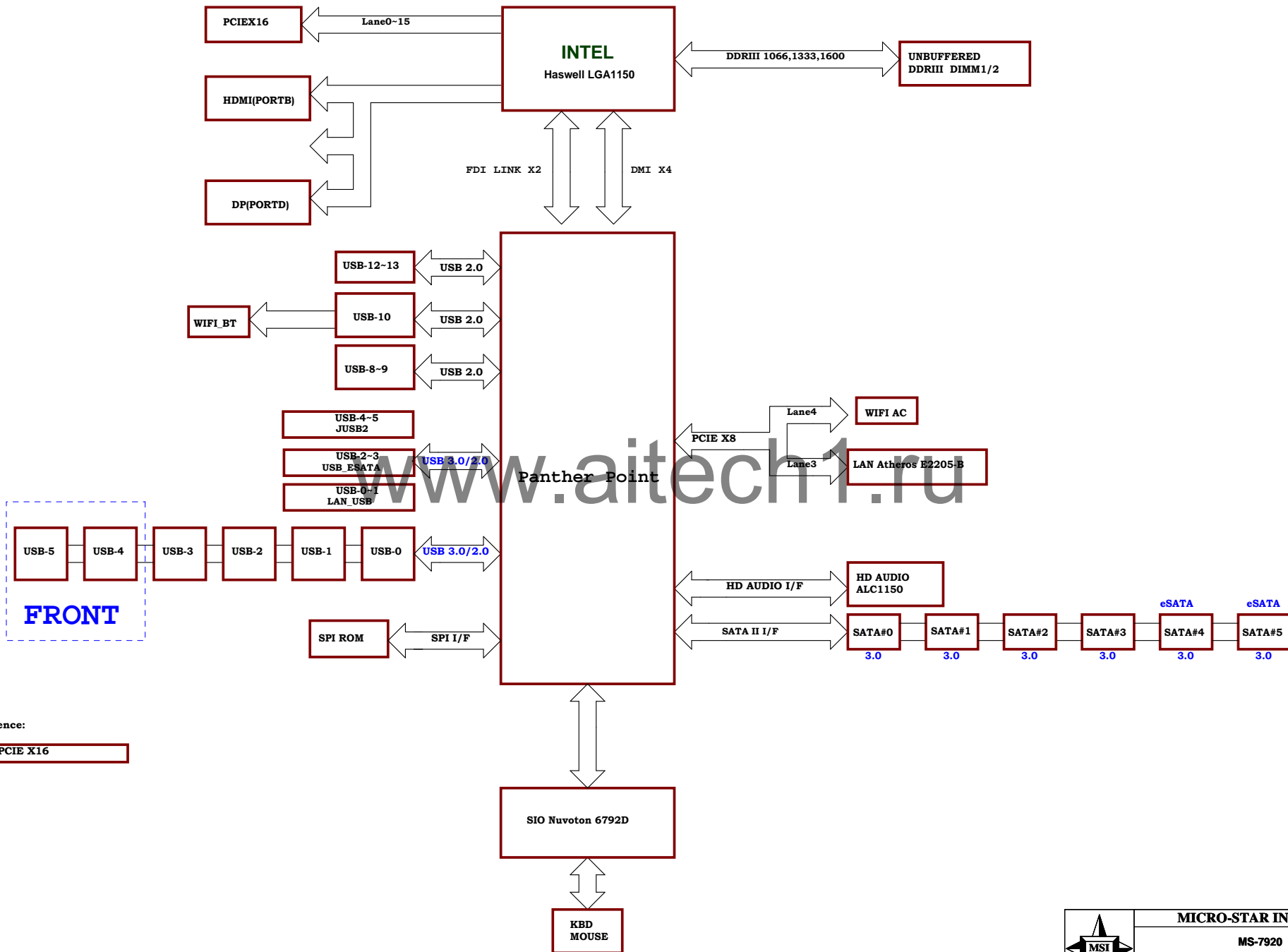
UP1649 6 Phase

Expansion Slots:

Other:

PCI Express (X16) Slot * 1

SATA3.0 x4(PCH)
ESATA x2(PCH)
REAL USB2.0 *4
FRONT USB2.0 *2
REAL USB3.0 *4
FRONT USB3.0 *2



Slot Sequence:

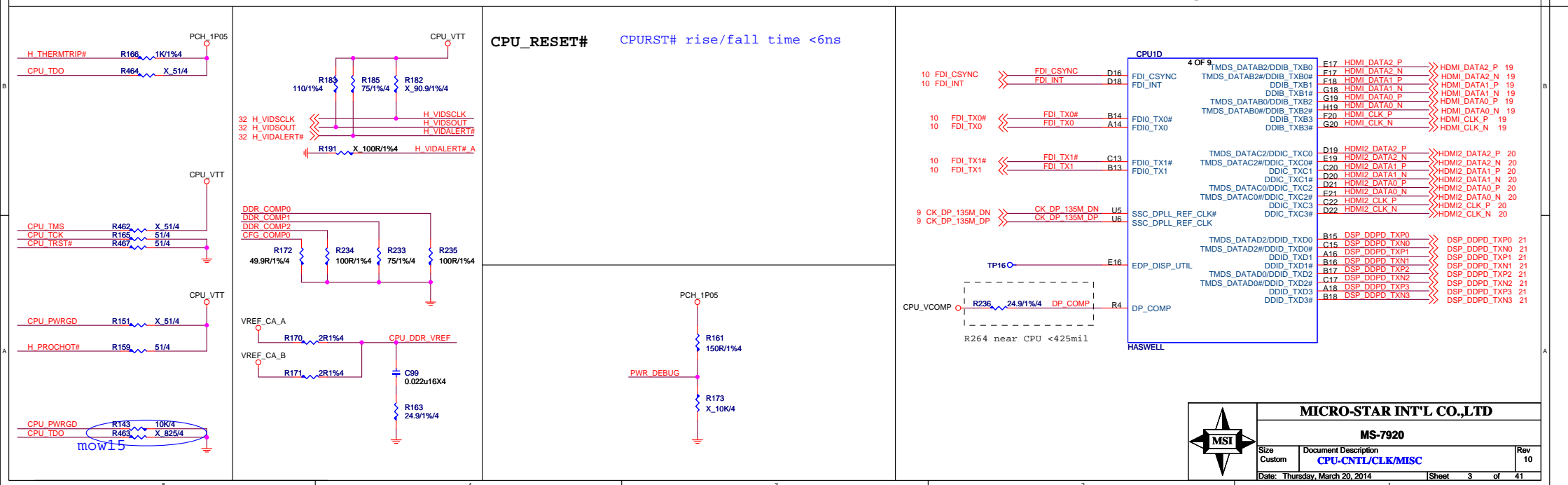
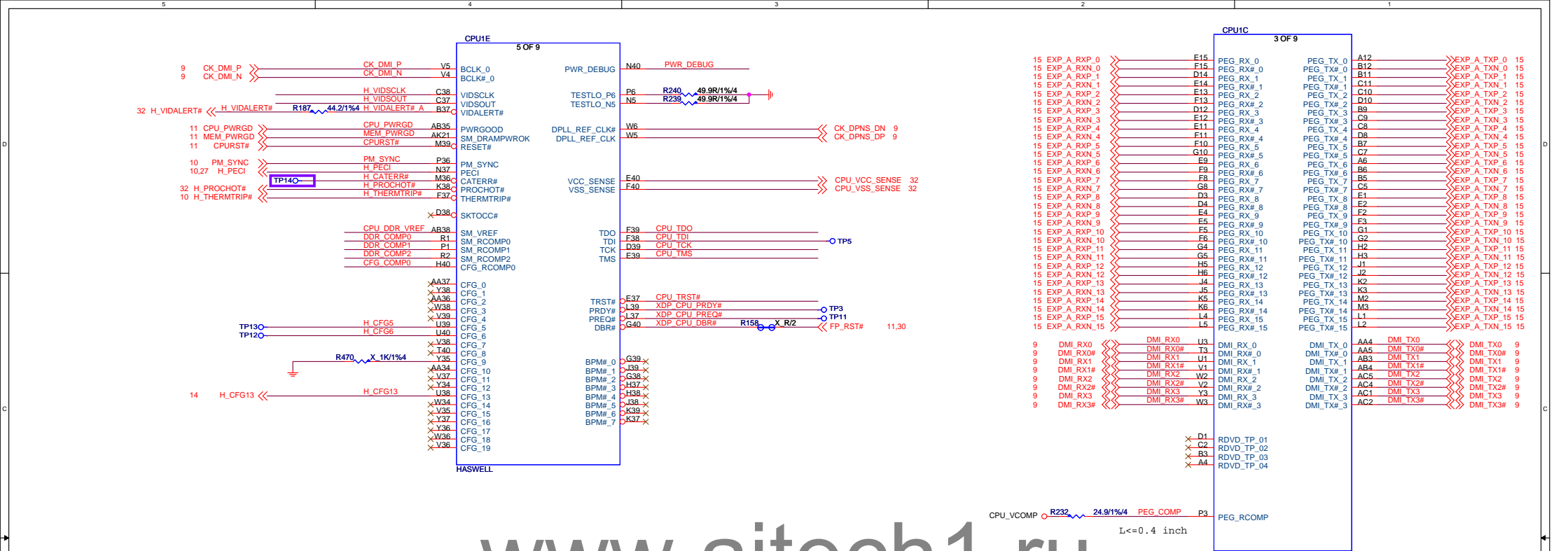
PCIE X16

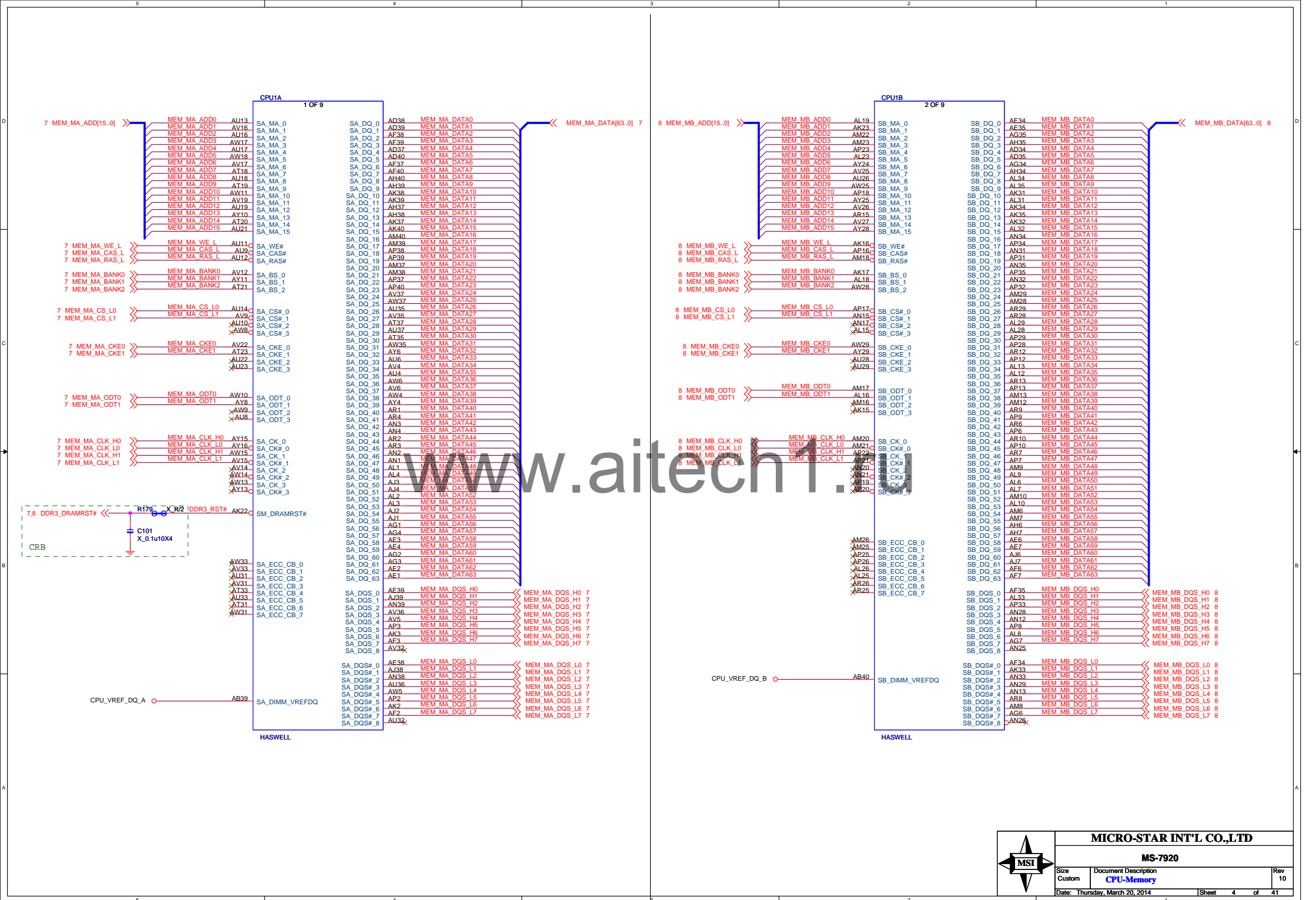


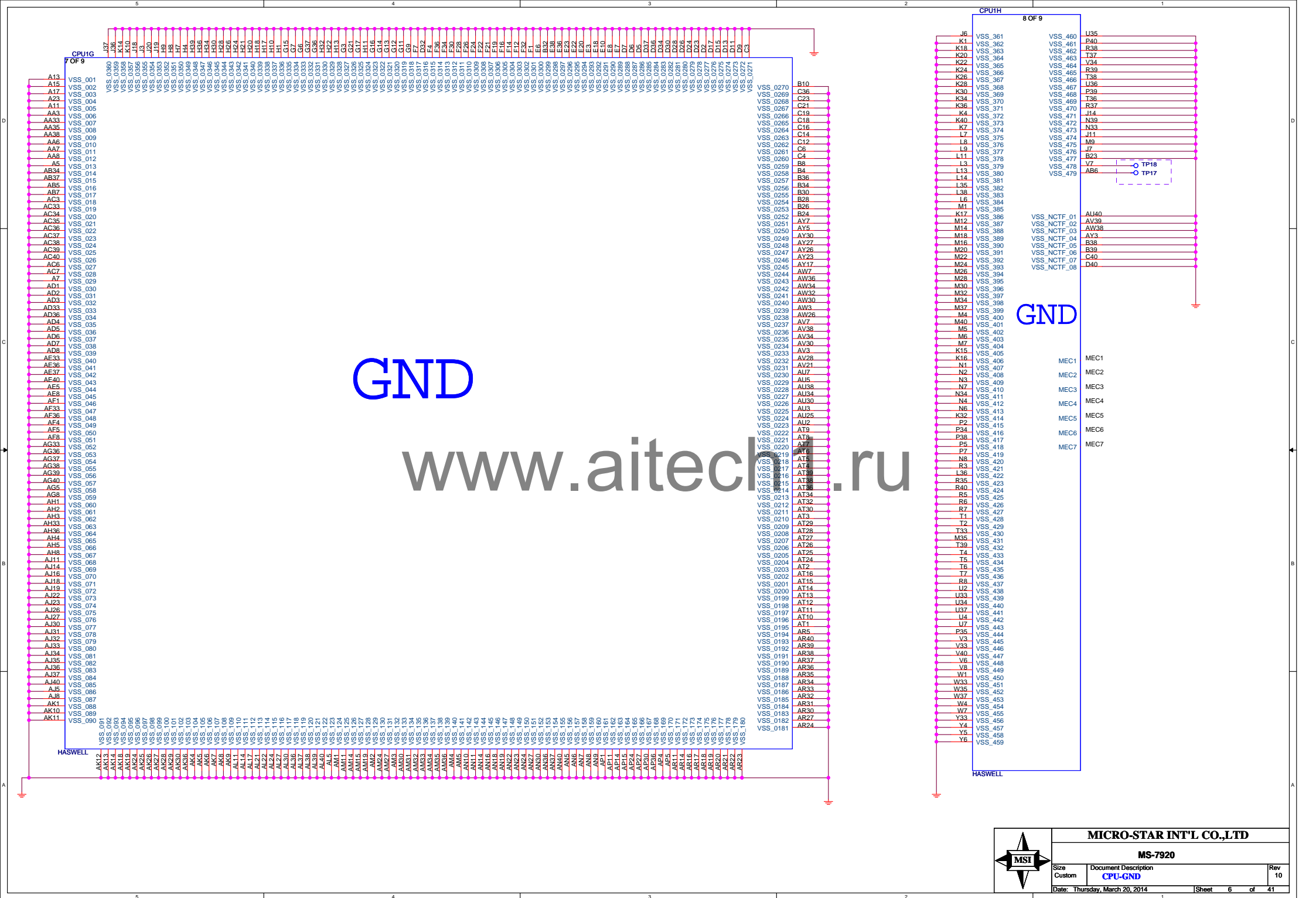
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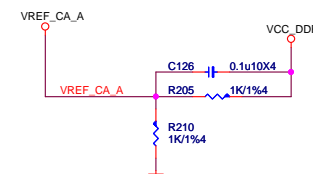
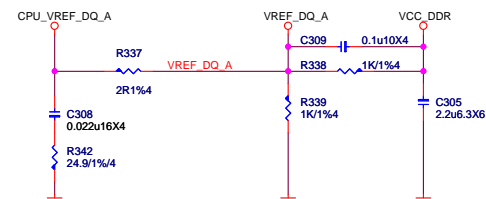
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VCC_DDR VCC3_SPD VTT_DDR



0x26:RH=18K,RL=13K

0x26:RH=18K,RL=13K



A0	B0

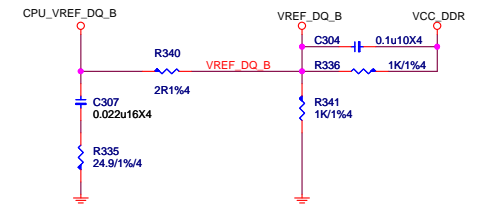
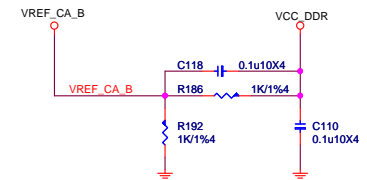
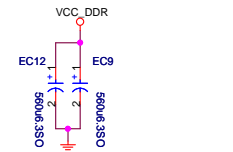
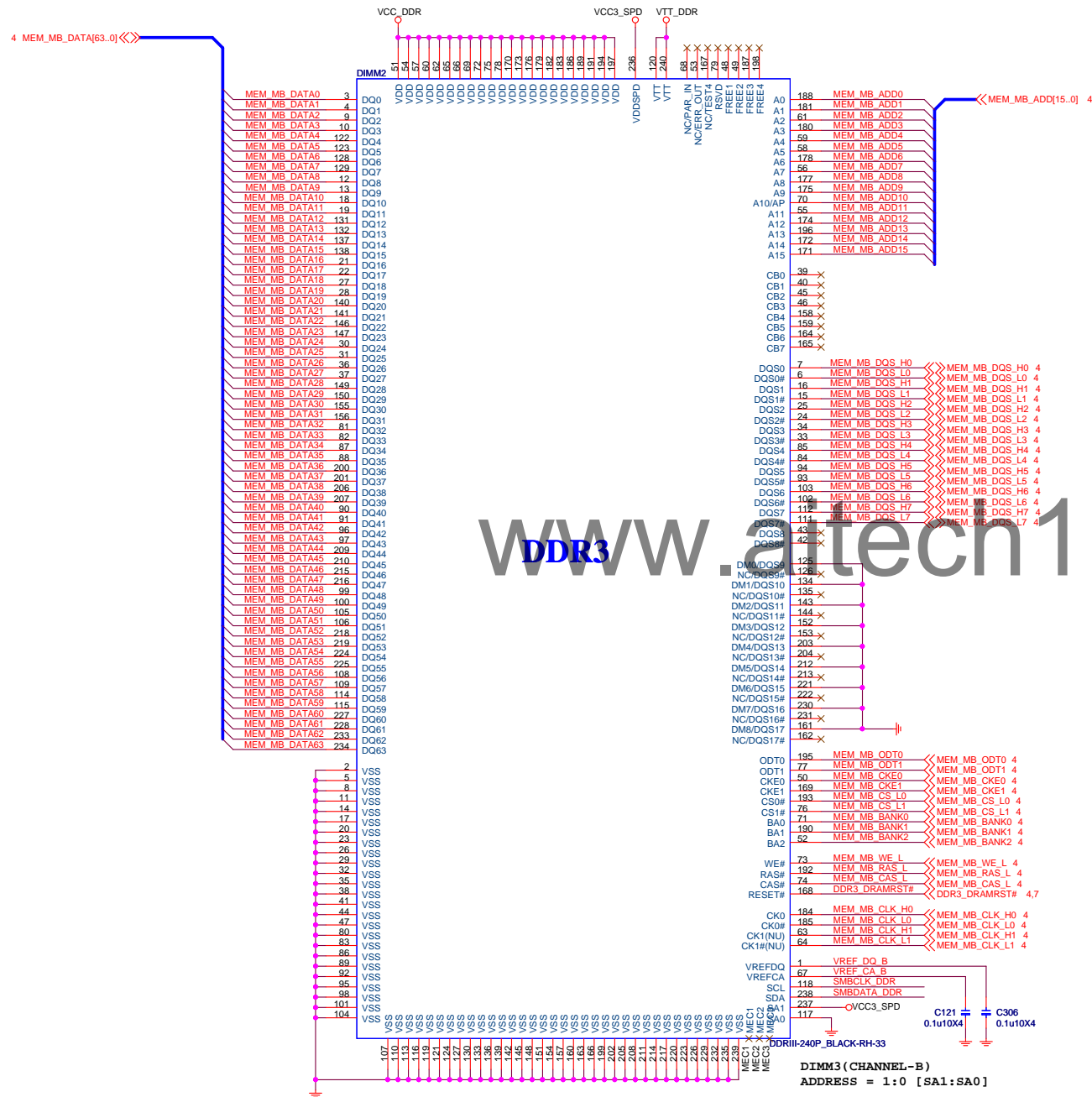
8 SMBCLK_DDR >> SMBCLK_DDR R532 33R/4 << SMBCLK_VCC 11,32

8 SMBDATA_DDR >> SMBDATA_DDR R533 33R/4 << SMBDATA_VCC 11,32

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DDRIII DIMM_B0



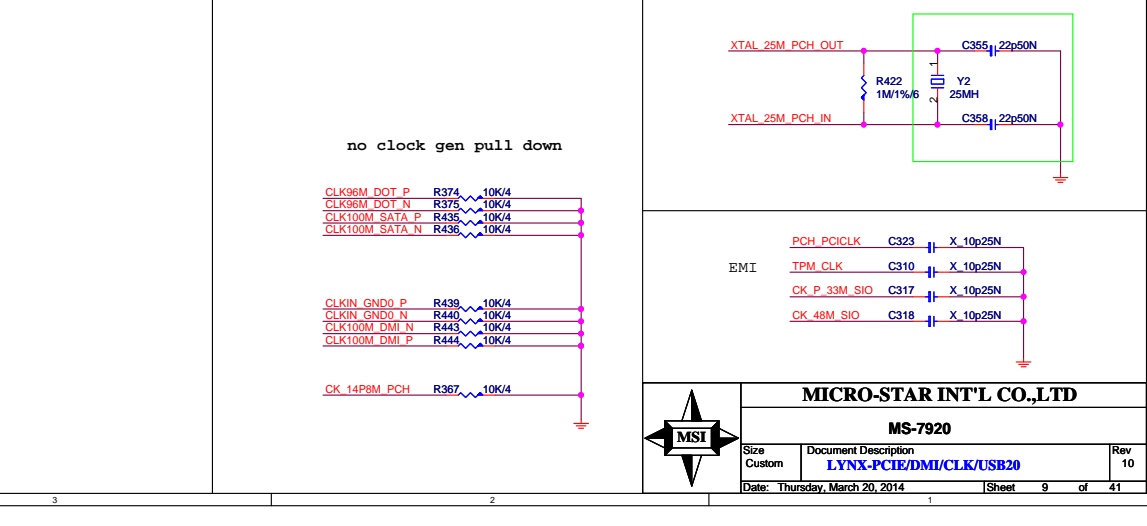
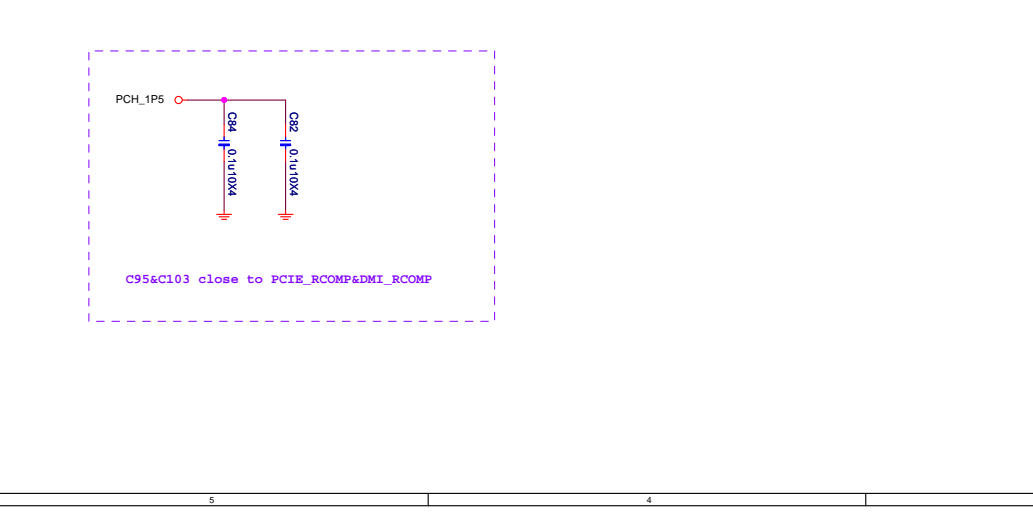
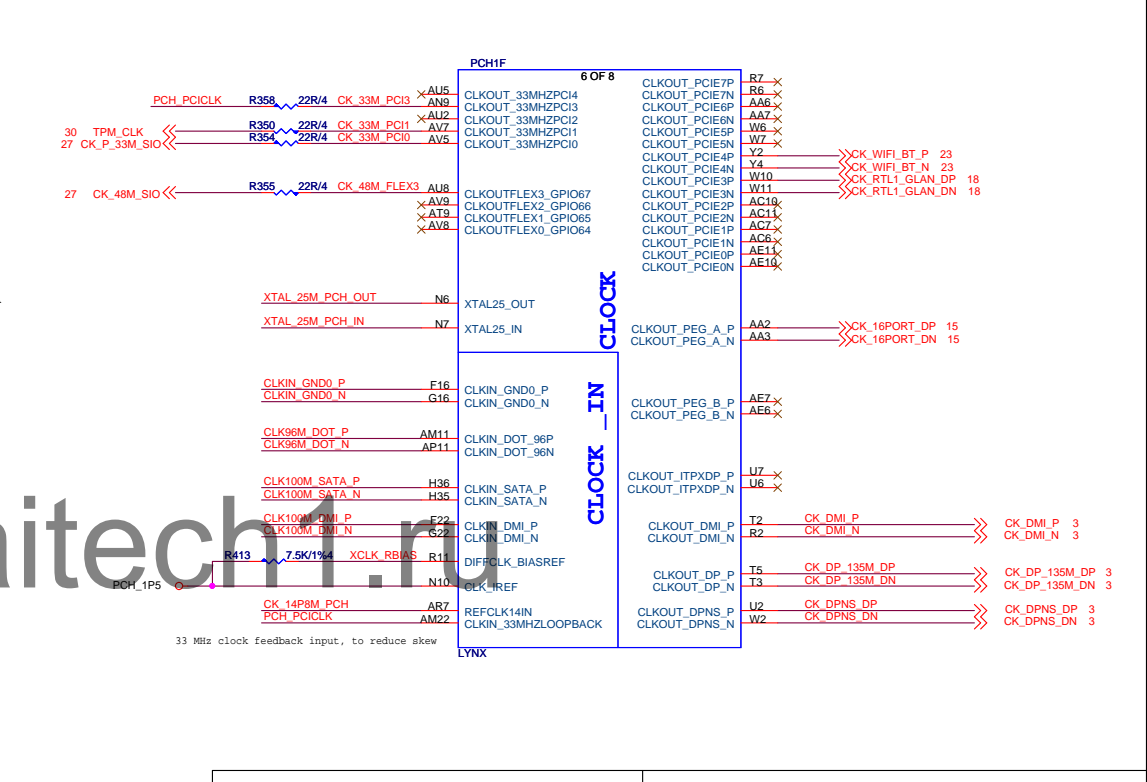
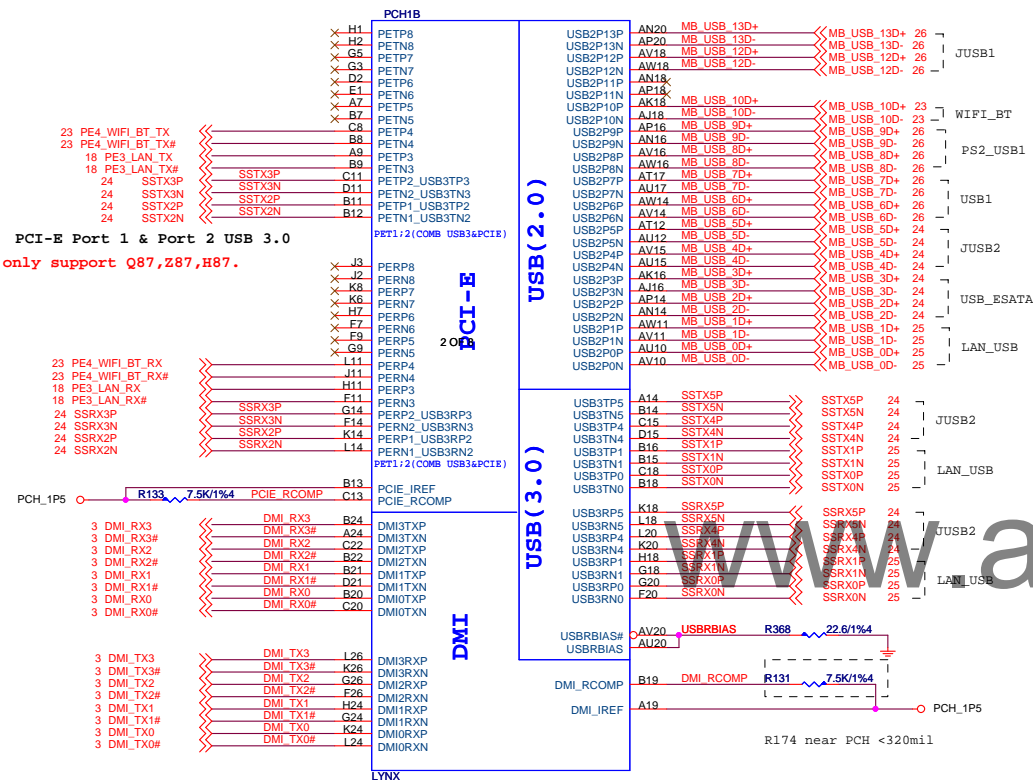
SMBCLK_DDR << SMBCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR 7

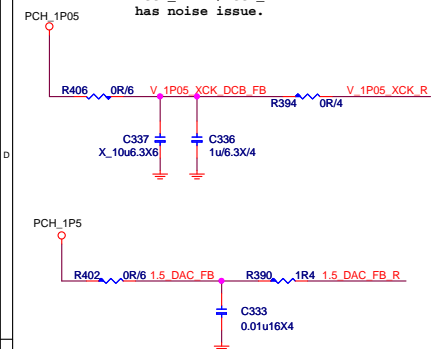


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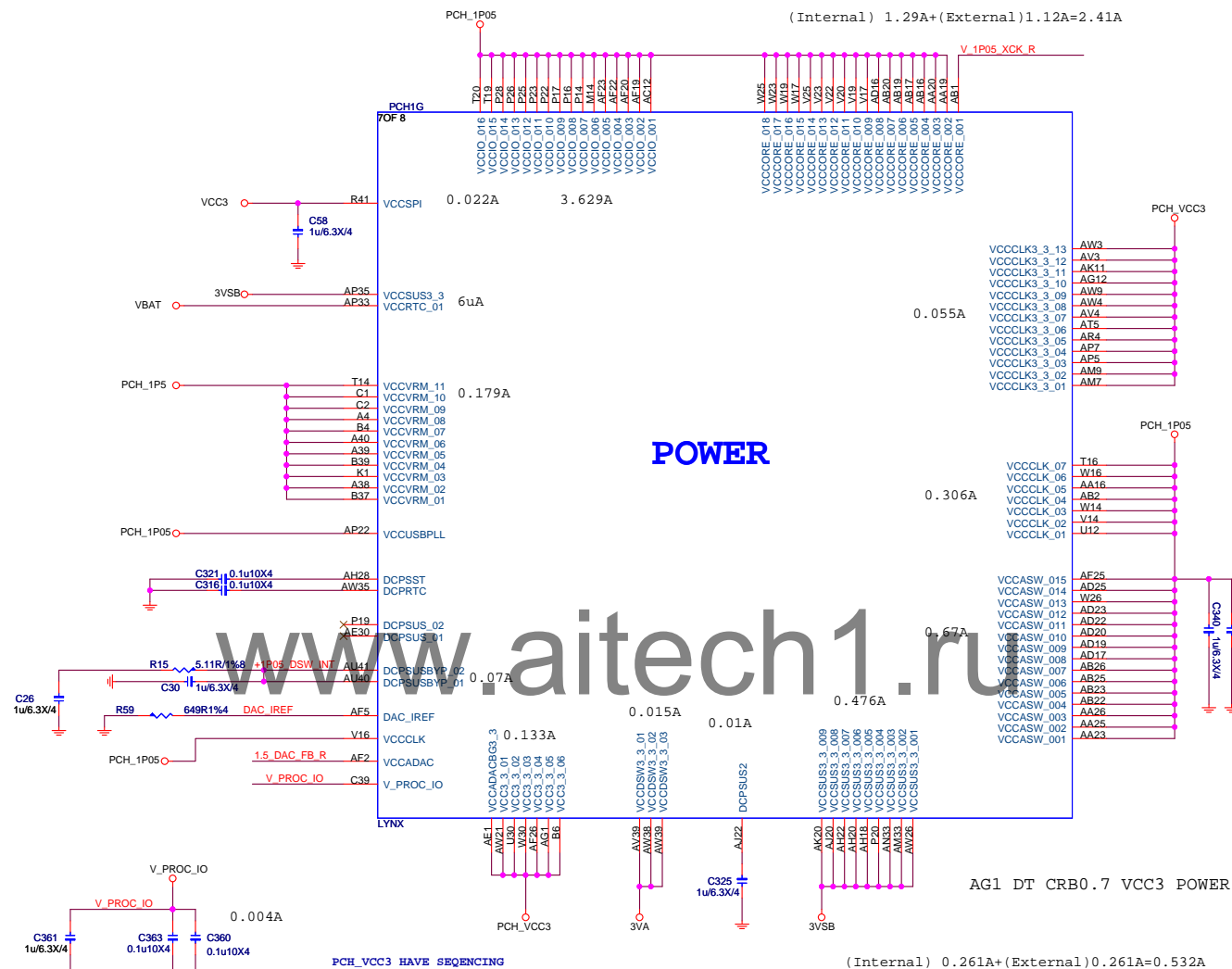
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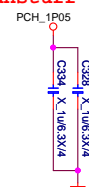


$$(\text{Internal}) \ 1.29A + (\text{External}) \ 1.12A = 2.41A$$


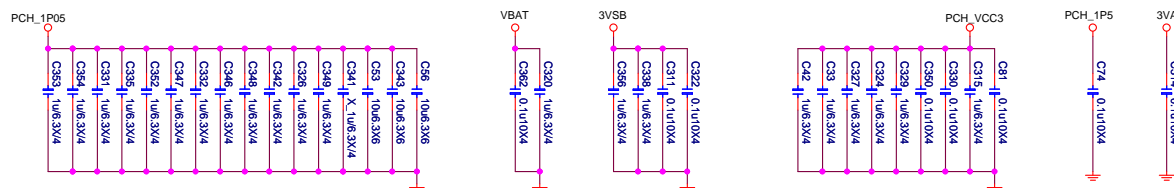
VCC3	0.21A
3VA	0.015A
VBAT	6uA
3VSB	0.261A
VCC1_5	0.249A
PCH 1P05	5.747A



Backside for V14,U12,T16,V16
unstuff



PCH decoupling cap



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Document Description
LYNX-POWE

Rev	10
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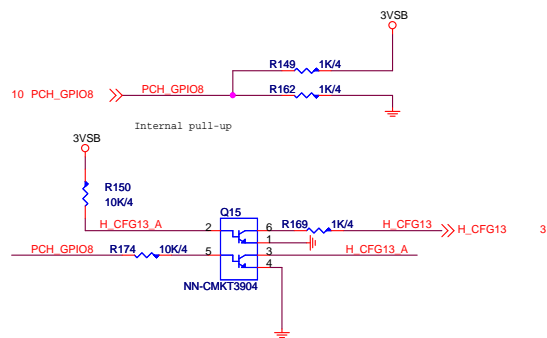
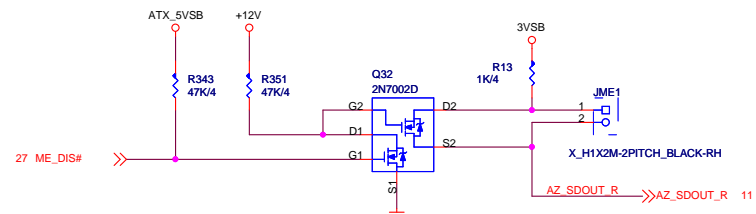
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--------------------------------	----------------

11,30 SPKR << SPKR R415 X 8.2K/4 PCH_VCC3

Internal pull-DOWN

SPKR
Default Mode:
Internal weak Pull-down.

No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



10 PCH_GPIO55 >> PCH_GPIO55 R420 X 4.7K/4

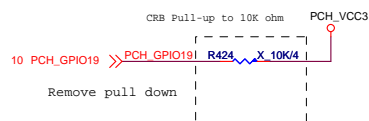
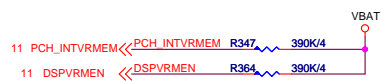
Internal pull-up

GPIO55
Default Mode:
Internal pull-up.

Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.

10 PCH_GPIO53 >> PCH_GPIO53 R23 X 1K/4

GPIO53
Connect to ground with 1k Ohm pull-down resistor.



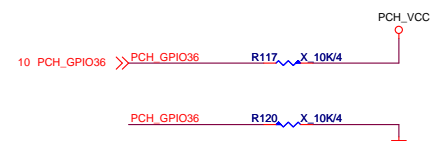
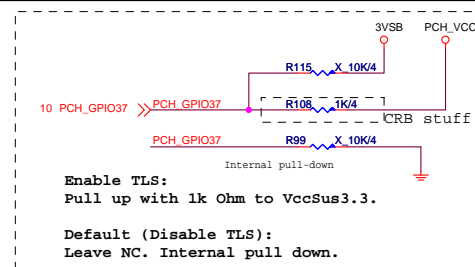
Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

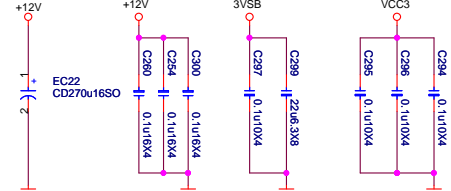
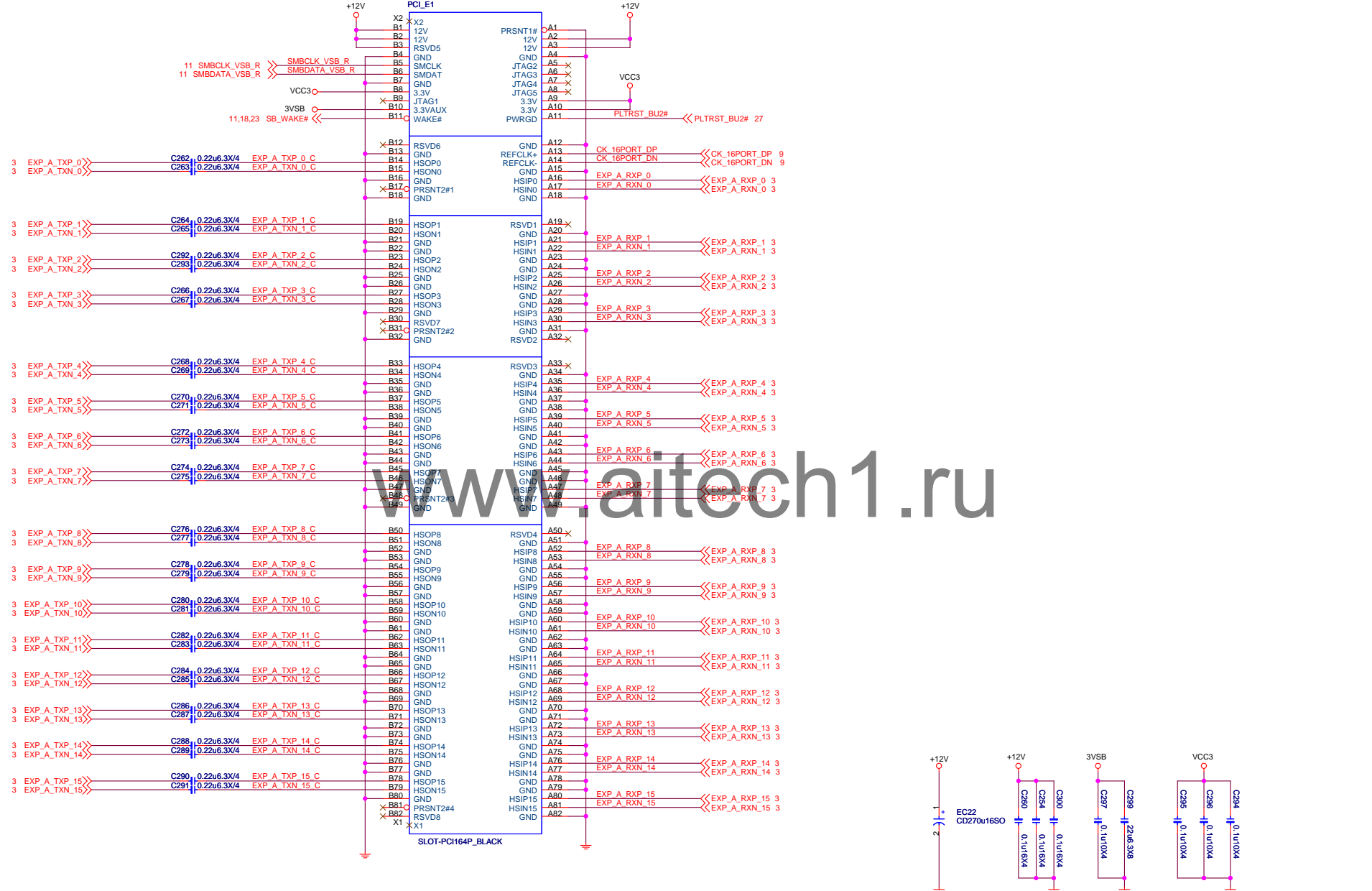
Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

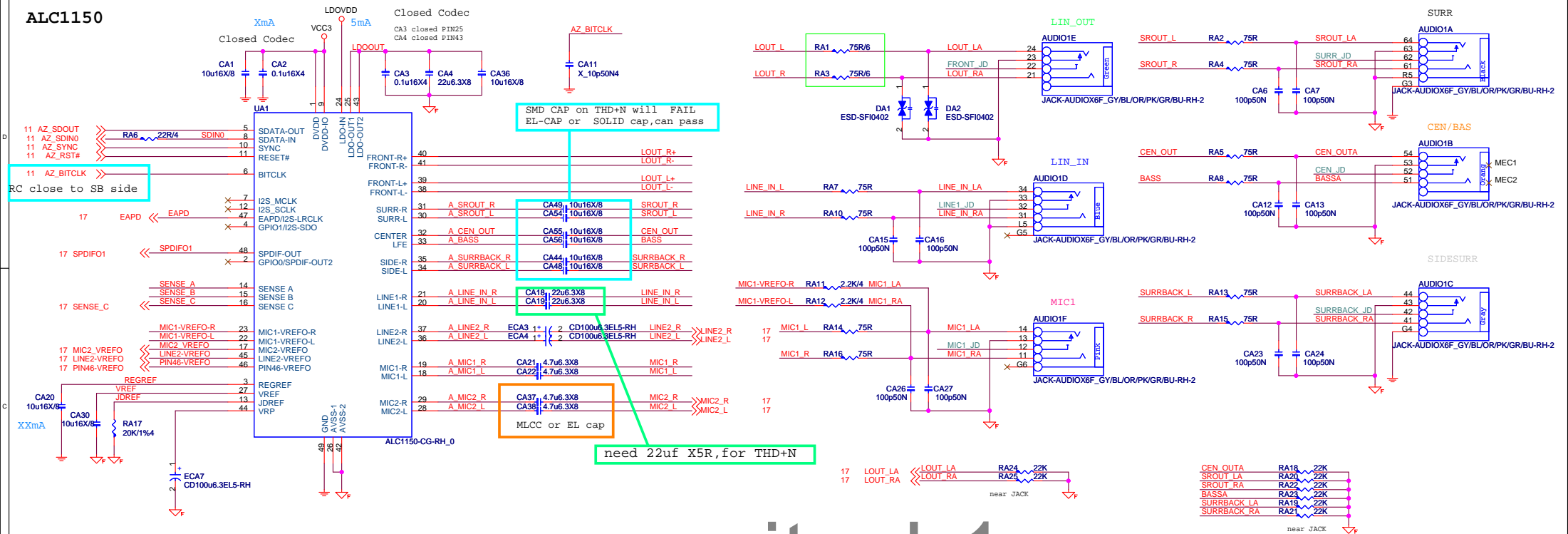
Default



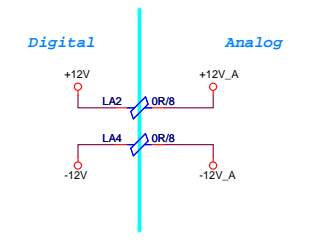
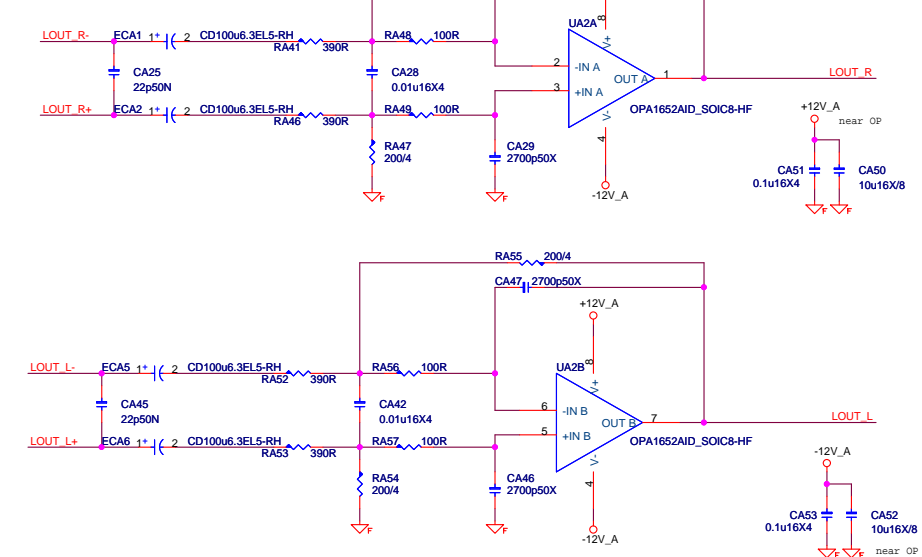
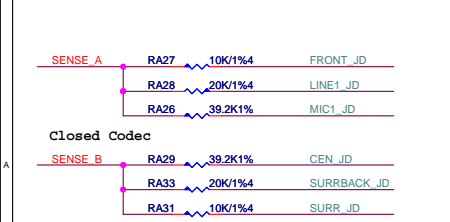
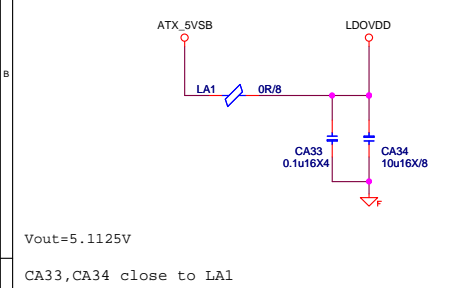
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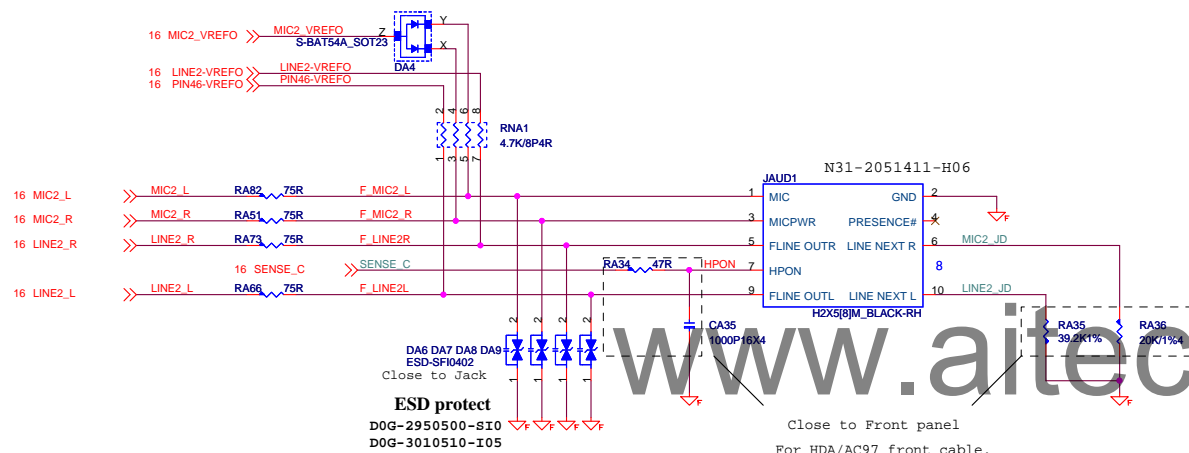
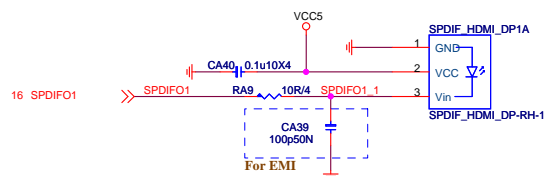
Size	Document Description	Rev
Custom	AUDIO 1150	10

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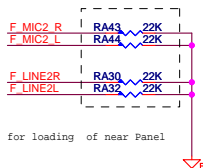
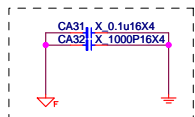
SPDIF OUT

N58-42M0021-F02 (HDMI+DP+SPDIF)
N58-06F0201-K06

AUDIO Moat LED

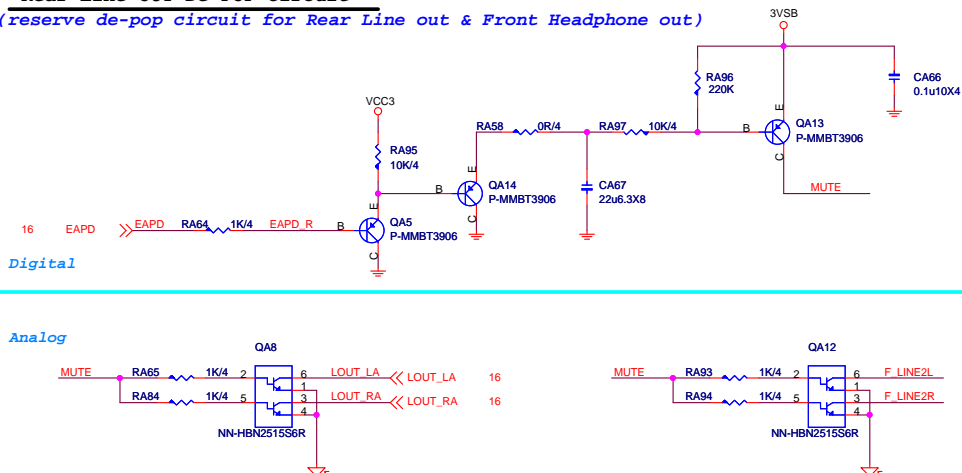


EMI



Rear Line OUT De-POP circuit

(reserve de-pop circuit for Rear Line out & Front Headphone out)

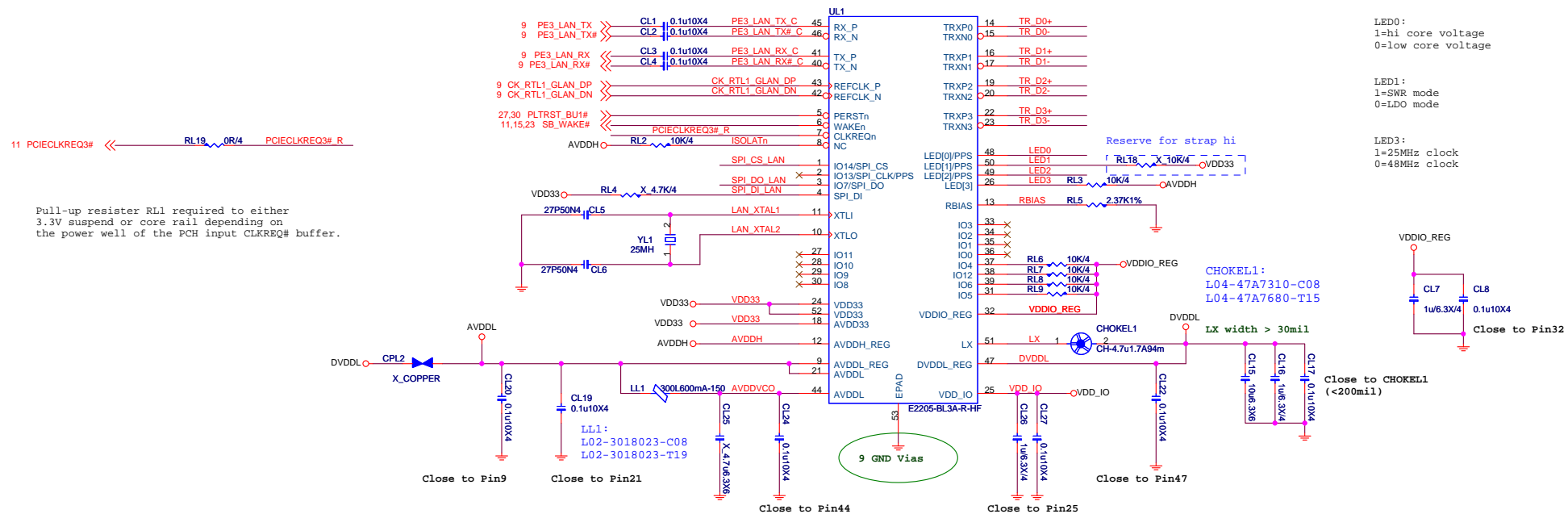


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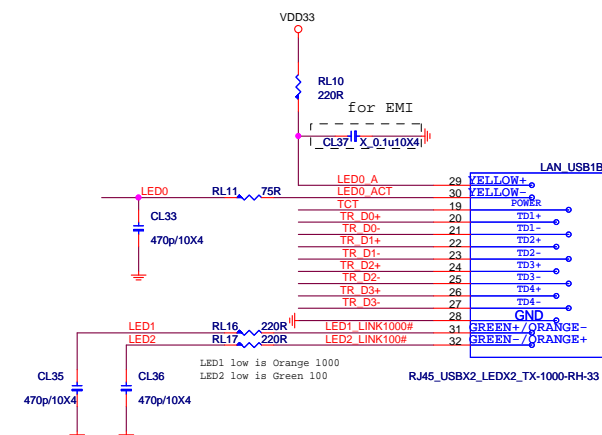
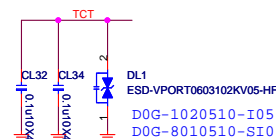
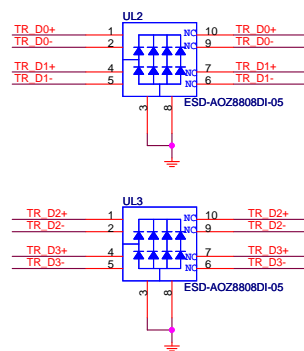
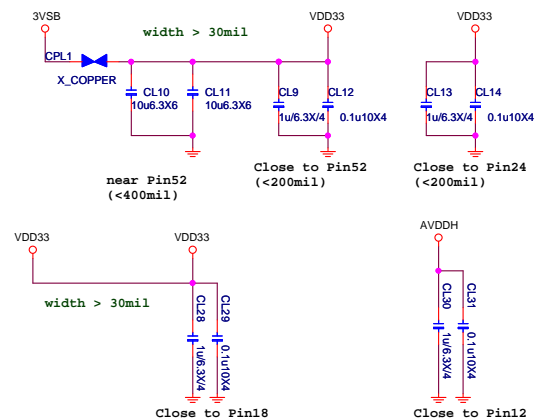
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E2205-B Giga LAN



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```
VDD33 power trace should be wider than 30mils;  
AVDD33 power trace should be wider than 30mils;  
VDD_IO power trace should be wider than 30mils;  
VDDIO_REG power trace should be wider than 20mils;  
AVDDH power trace should be wider than 20mils;  
AVDDL power traces should be wider than 20mils.  
DVDDL power traces should be wider than 20mils.
```



- ```

10:
1. Support xD, not support SPI
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFUS
01:
1. Support SPI, not support xD
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFUS
11:
1. Not support xD, not support SPI
2. Only support PPS, PPS always at CRI013.

```

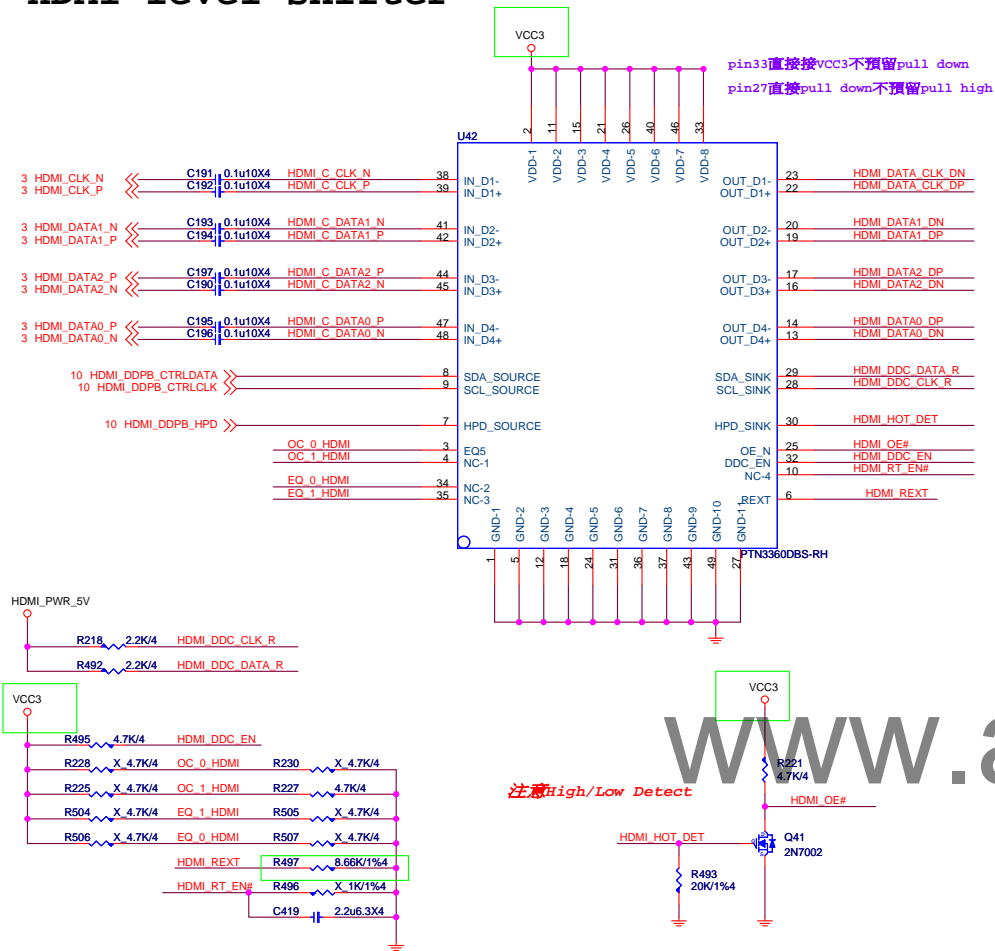


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**MS-7920**

|                                |                                                      |                |
|--------------------------------|------------------------------------------------------|----------------|
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# HDMI level shifter



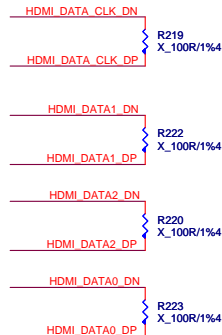
|           | "0"                                                          | "1"                                                                               |
|-----------|--------------------------------------------------------------|-----------------------------------------------------------------------------------|
| DDC_EN    | DDC level shifter disable                                    | DDC level shifter enable                                                          |
| RT_EN#    | Input 50 ohm termination resistor enable                     | the input termination ; resistors are set to high impedances                      |
| OE#       | enable                                                       | the chip is power down and input termination resistors will be at high impedance. |
| HPD_SINK  | disable                                                      | enable                                                                            |
| DDCBUF_EN | For DDC level shifting configuration, please refer to Table. |                                                                                   |
| REXT      |                                                              |                                                                                   |

| [DDC_EN, DDCBUF_EN, OE#] | DDC Passive Switch | DDC Active Buffer |
|--------------------------|--------------------|-------------------|
| 1, 0, X                  | On                 | Off               |
| 1, 1, 0                  | Off                | On                |
| 1, 1, 1                  | Off                | Off               |
| 0, X, X                  | Off                | Off               |

| PC1, PC0 |       | note                             |
|----------|-------|----------------------------------|
| 00       | 8 dB  | internal pull-down at ~500K ohm. |
| 01       | 4 dB  |                                  |
| 10       | 12 dB |                                  |
| 11       | 0 dB  |                                  |

note  
internal pull-up at ~500K ohm.  
internal pull-down at ~500K ohm.  
internal pull-down at ~500K ohm.  
internal pull-down at ~200K ohm; 5V tolerant.  
internal pull-down at ~500K ohm.  
analog current generation.

## EMI



## EMI cap.

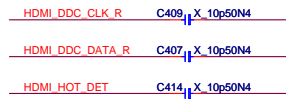
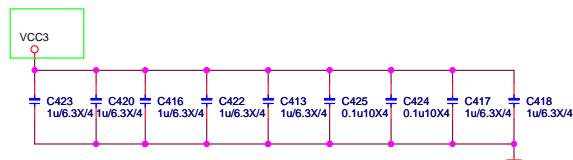
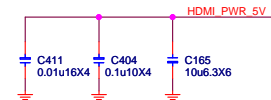
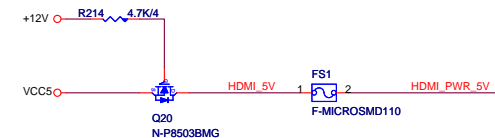
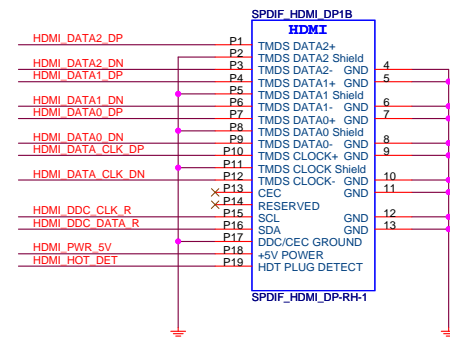


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

| Port   | Digital Display Interface Differential Pairs | HDMI Signals    | PCH Digital Display Interface Pins   |
|--------|----------------------------------------------|-----------------|--------------------------------------|
| Port B | DDSP_B_TX0_DN                                | TMDSB_DATA2#    | DDPB_0N                              |
|        | DDSP_B_TX0_DP                                | TMDSB_DATA2     | DDPB_0P                              |
|        | DDSP_B_TX1_DN                                | TMDSB_DATA1#    | DDPB_1N                              |
|        | DDSP_B_TX1_DP                                | TMDSB_DATA1     | DDPB_1P                              |
|        | DDSP_B_TX2_DN                                | TMDSB_DATA0#    | DDPB_2N                              |
|        | DDSP_B_TX2_DP                                | TMDSB_DATA0     | DDPB_2P                              |
|        | DDSP_B_TX3_DN                                | TMDSB_CLK#      | DDPB_3N                              |
|        | DDSP_B_TX3_DP                                | TMDSB_CLK       | DDPB_3P                              |
|        | DDPB_HPDP                                    | DDSPB_HPD0      | Hot plug detect used by HDMI Port B. |
|        | SDVO_CTRLCLK                                 | HDMI8_CTRL_CLK  | HDMI DDC lines for Port B            |
|        | SDVO_CTRLDATA                                | HDMI8_CTRL_DATA |                                      |
|        |                                              |                 |                                      |

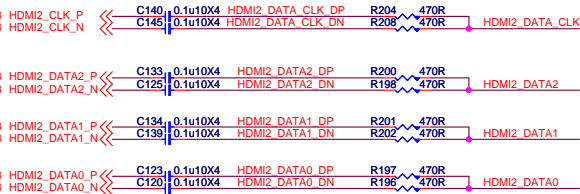


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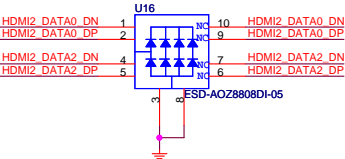
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| Custom | HDMI Connector           | 10             |
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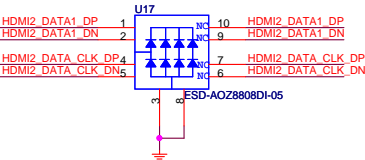
HDMI Cost Reduced Level Shifter



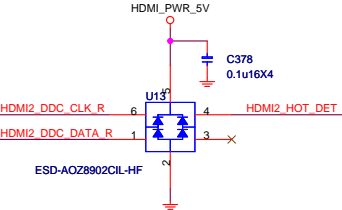
U1 AVL:D0G-05A050C-005  
D0G-06A050C-A68



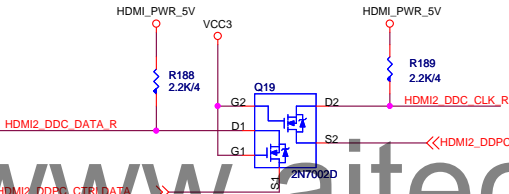
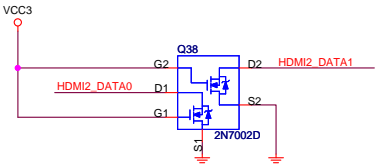
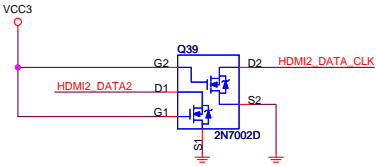
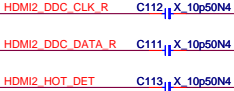
U75 AVL:D0G-05A050C-005  
D0G-06A050C-A68



U2 AVL:D0G-0100619-I05



EMI cap.



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HPD

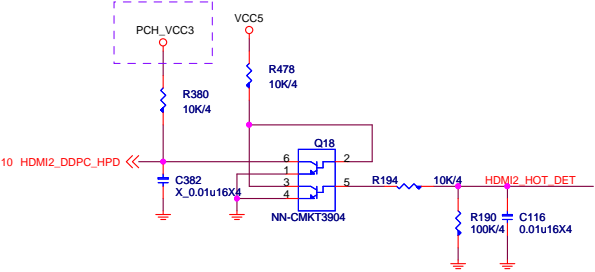
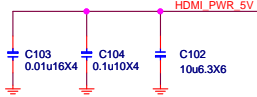
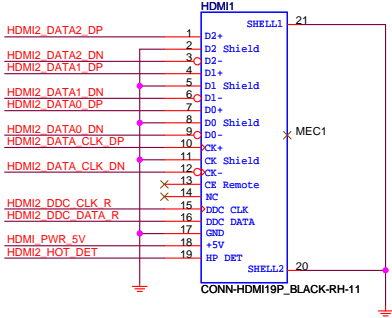
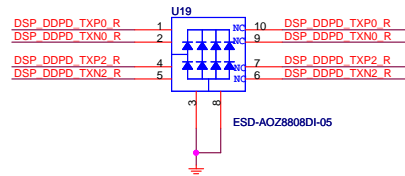


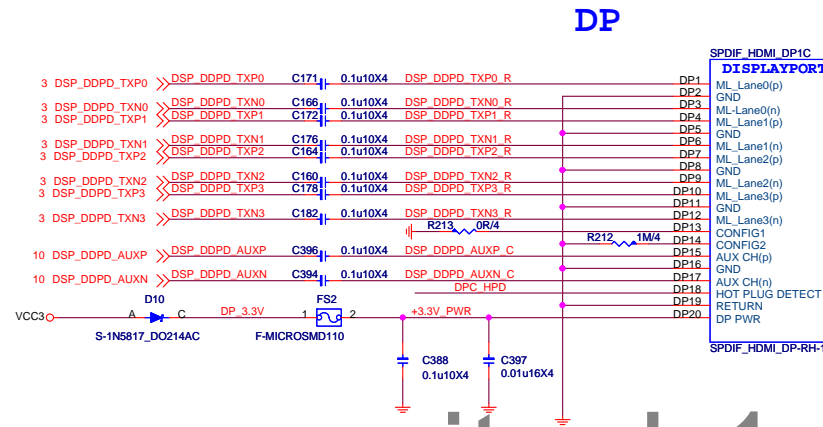
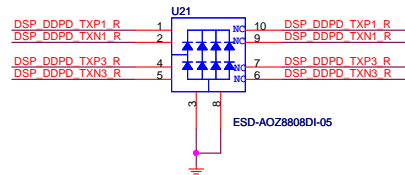
Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

| Port   | Digital Display Interface Differential Pairs | HDMI Signals     | PCH Digital Display Interface Pins   |
|--------|----------------------------------------------|------------------|--------------------------------------|
| Port B | DDSP_B_TX0_DN                                | TMDSB_DATA2#     | DDPB_ON                              |
|        | DDSP_B_TX0_DP                                | TMDSB_DATA2      | DDPB_OP                              |
|        | DDSP_B_TX1_DN                                | TMDSB_DATA1#     | DDPB_1N                              |
|        | DDSP_B_TX1_DP                                | TMDSB_DATA1      | DDPB_1P                              |
|        | DDSP_B_TX2_DN                                | TMDSB_DATA0#     | DDPB_2N                              |
|        | DDSP_B_TX2_DP                                | TMDSB_DATA0      | DDPB_2P                              |
|        | DDSP_B_TX3_DN                                | TMDSB_CLK#       | DDPB_3N                              |
|        | DDSP_B_TX3_DP                                | TMDSB_CLK        | DDPB_3P                              |
|        | DDPB_HPDP                                    | DDSP_B_HPDP0     | Hot plug detect used by HDMI Port B. |
|        | SDVO_CTRLCLK                                 | HDMI_B_CTRL_CLK  | HDMI DDC lines for Port B            |
|        | SDVO_CTRLDATA                                | HDMI_B_CTRL_DATA |                                      |

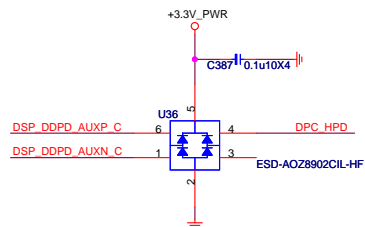




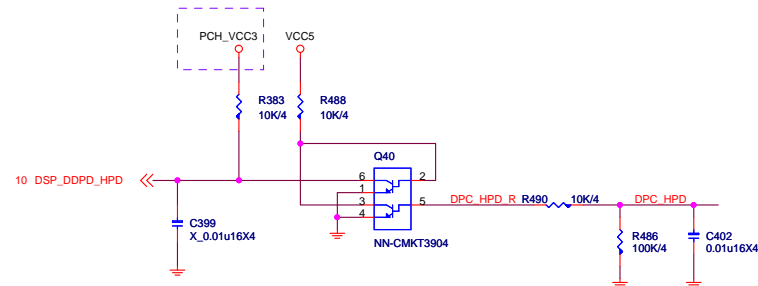
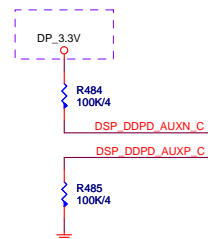
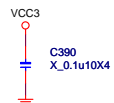
AVL:D0G-06A050C-A68



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D0G-0200529-A68 Main  
D0G-0100619-I05 AVL



MICRO-STAR INT'L CO.,LTD

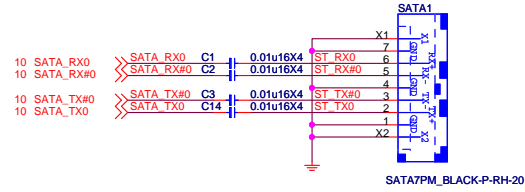
MS-7920

|        |                          |                |
|--------|--------------------------|----------------|
| Size   | Document Description     | Rev            |
| Custom | DISPLAY Connector        | 10             |
| Date:  | Thursday, March 20, 2014 | Sheet 21 of 41 |

SATA port  
Z87,H87:Port 0 ~ 5 are SATA 6G  
B85: Port 0, 1, 2, 3 are SATA 6G  
H81: Port 0, 1 are SATA 6G  
B85,H81: Port 4,5 are SATA 3G

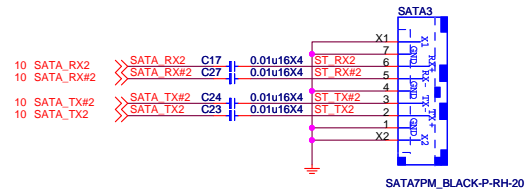
### SATA 6G PORT 0,1

3.0 BLACK



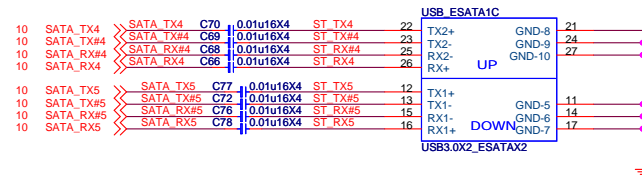
### SATA 6G PORT 2,3

3.0 BLACK



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### eSATA 6G PORT 4

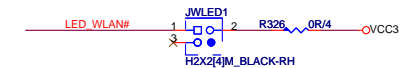
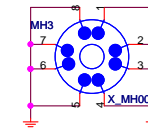
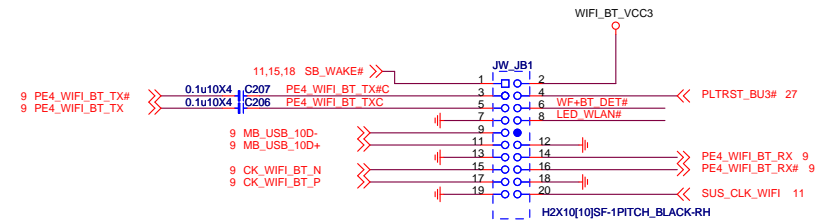
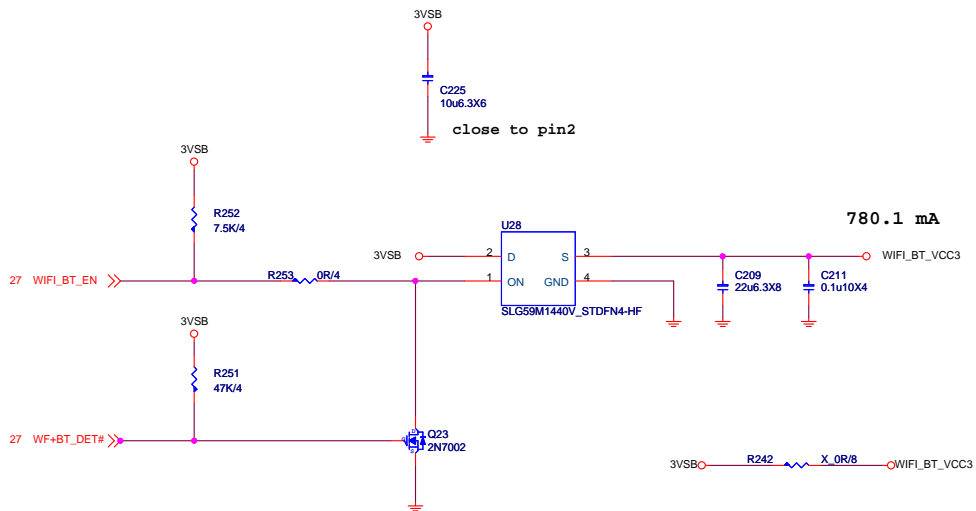


MICRO-STAR INT'L CO.,LTD

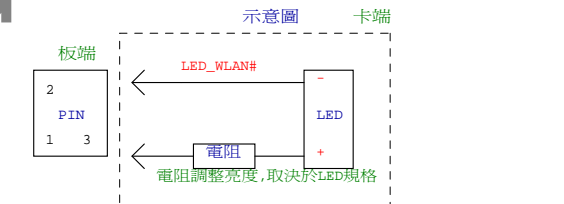
MS-7920

|                                |                      |     |
|--------------------------------|----------------------|-----|
| Size                           | Document Description | Rev |
| Custom                         | SATA Connector       | 10  |
| Date: Thursday, March 20, 2014 | Sheet 22 of 41       |     |





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MS-7920

| Size                           | Document Description | Rev |
|--------------------------------|----------------------|-----|
| Custom                         | WIFI connector       | 10  |
| Date: Thursday, March 20, 2014 | Sheet 23 of 41       |     |

(OC2#)

Diagram illustrating the connection of the CMC-L12-9008080-HF module to the MB\_USB\_4D+ and MB\_USB\_4D- signals.

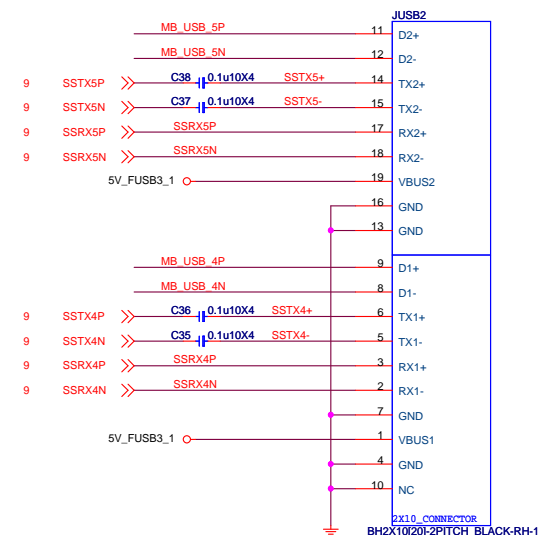
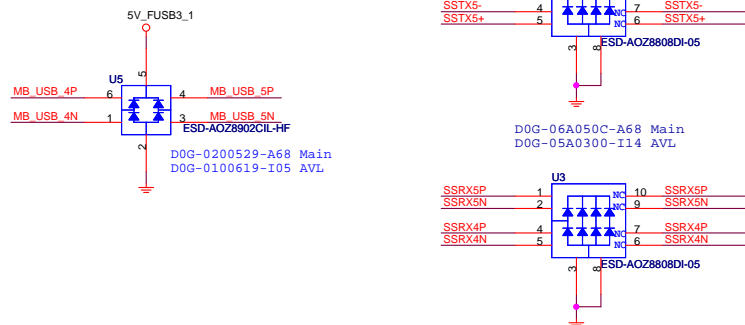
The module is connected to the MB\_USB\_4D+ signal (pin 4) and the MB\_USB\_4D- signal (pin 3). The module output is connected to the MB\_USB\_4P signal (pin 1) and the MB\_USB\_4N signal (pin 2).

Diagram illustrating the connection of the CMC-L12-9008080-HF module to the MB\_USB\_5D+ and MB\_USB\_5D- signals.

The module is connected to the MB\_USB\_5D+ signal (pin 4) and the MB\_USB\_5D- signal (pin 3). The module output is connected to the MB\_USB\_5P signal (pin 1) and the MB\_USB\_5N signal (pin 2).

CMC:

- L12-9008080-P01
- L12-9008090-M09
- L12-9008100-I05
- L12-9008110-T34



(OC1#)

9 MB\_USB\_2D+ >> MB\_USB\_2D+ 4 1 MB\_USB\_2P

9 MB\_USB\_2D- >> MB\_USB\_2D- 3 2 MB\_USB\_2N

L5 CMC-L12-9008080-HF

9 MB\_USB\_3D+ >> MB\_USB\_3D+ 4 1 MB\_USB\_3P

9 MB\_USB\_3D- >> MB\_USB\_3D- 3 2 MB\_USB\_3N

L3 CMC-L12-9008080-HF

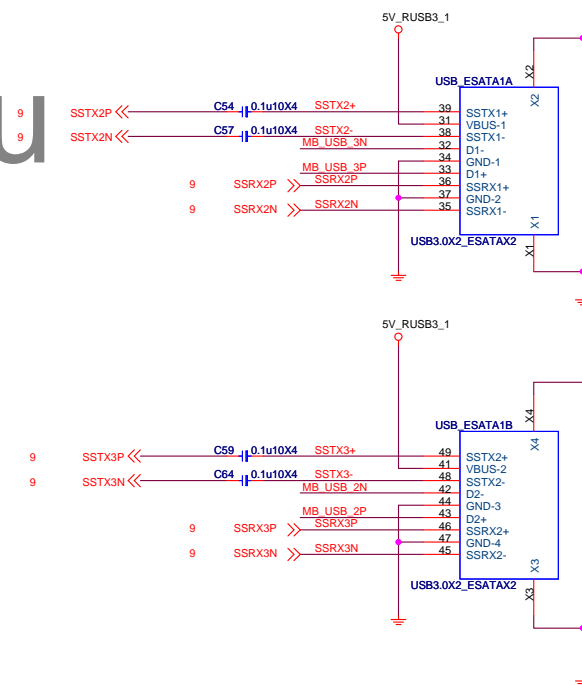
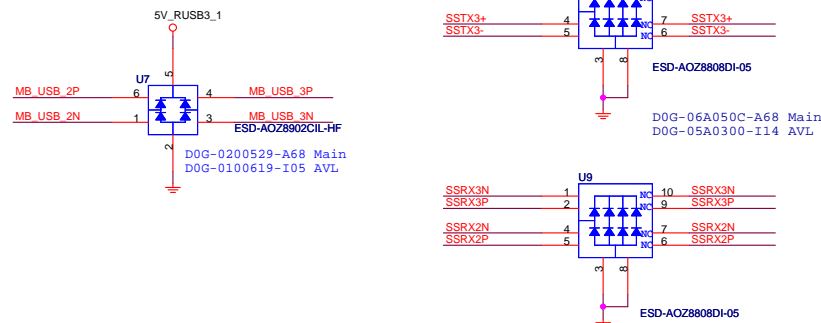
CMC:

L12-9008080-P01

L12-9008090-M09

L12-9008100-I05

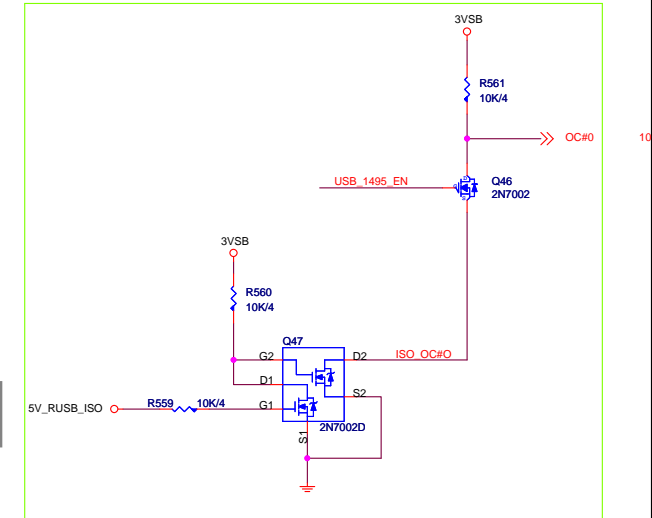
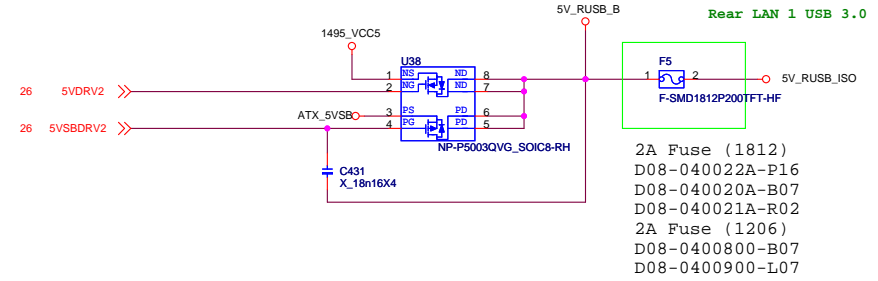
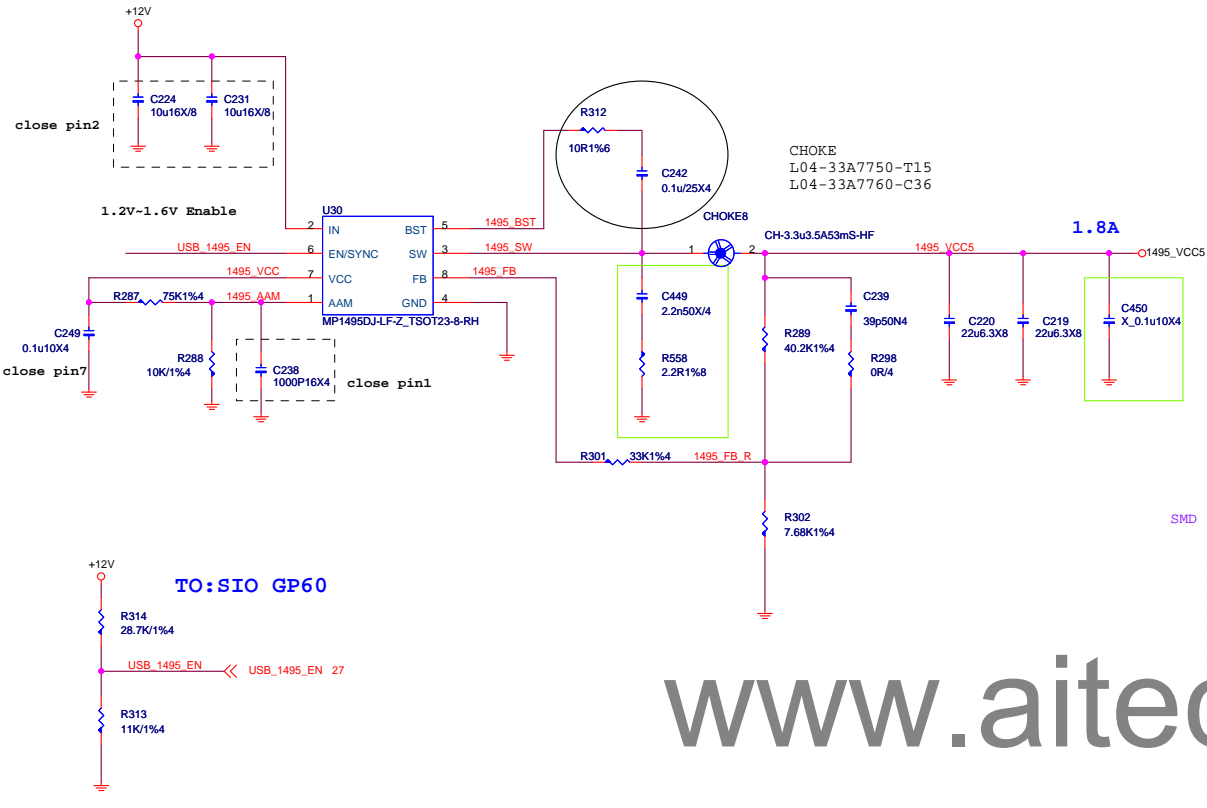
L12-9008110-T34

**MS-7920**

|                                |                                                 |                |
|--------------------------------|-------------------------------------------------|----------------|
| Size<br>Custom                 | Document Description<br><b>USB3.0 connector</b> | Rev<br>10      |
| Date: Thursday, March 20, 2014 |                                                 | Sheet 24 of 41 |

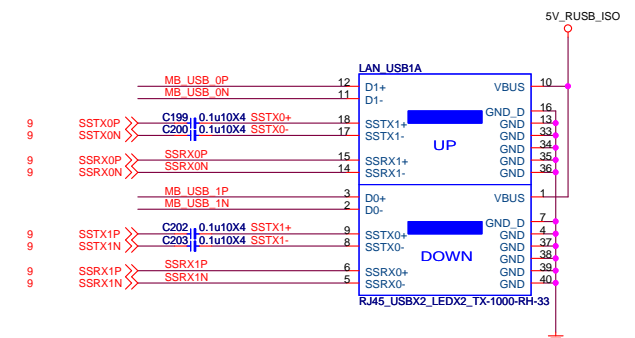
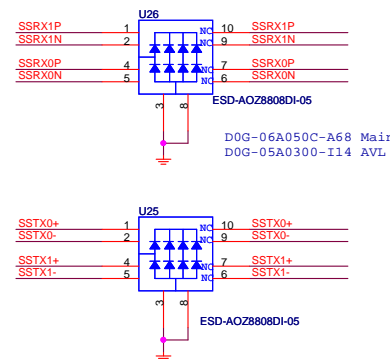
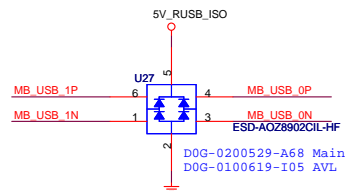
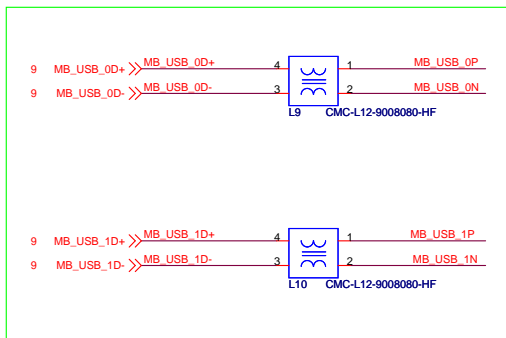
# LAN USB Power (OC0#)

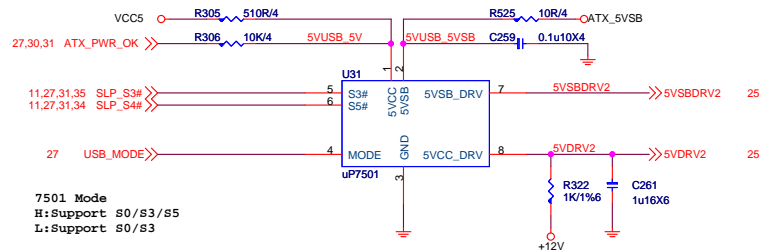
OCF:4.2-5A  
frequency:500KHz



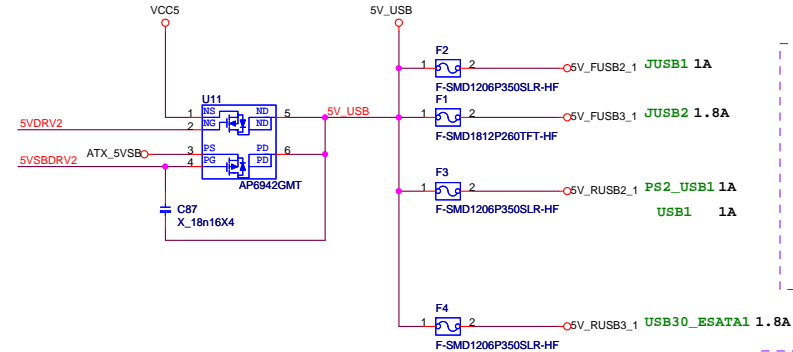
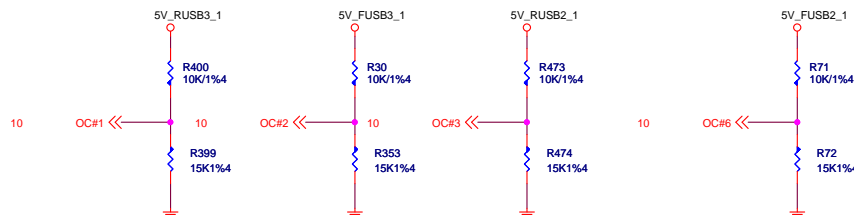
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CMC:  
L12-9008080-P01  
L12-9008090-M09  
L12-9008100-I05  
L12-9008110-T34  
CMC Stuff 0R:R3C-0000012-W08



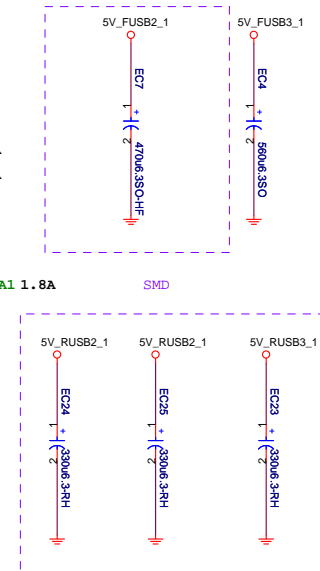


5VDRV2, 5VSBDRV2 width 12mil



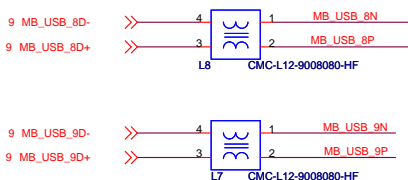
背板限高3mm, 才改用330u

F2:D08-0300700-P16 (Itrip=2.6A; 0.015ohm)  
F1.F4.F6:D08-2000300-P16 (Itrip=3.5A; 0.003ohm)

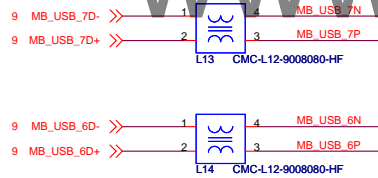


#### REAR USB PORT 08,09 (With Ps2) (OC4#)

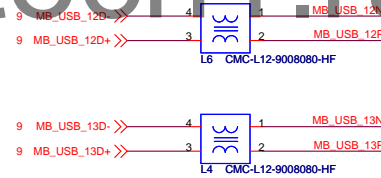
CMC Stuff 0R:R3C-0000012-W08



#### REAR USB PORT 6,7 (OC3#)

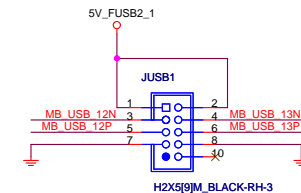
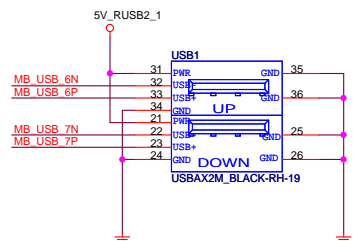
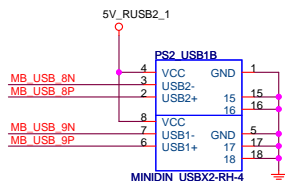
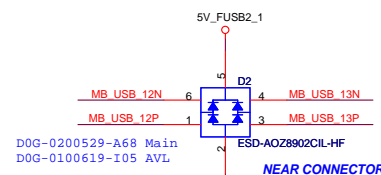
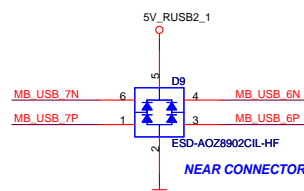
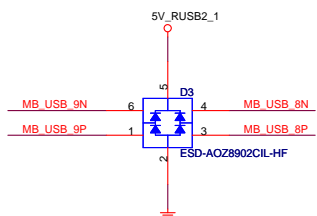
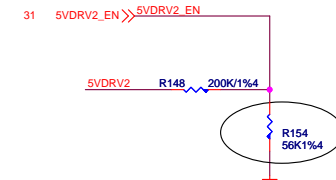


#### FRONT USB PORT 12,13 (OC6#)



CMC:  
L12-9008080-P01  
L12-9008090-M09  
L12-9008100-I05  
L12-9008110-T34

#### USB MODE



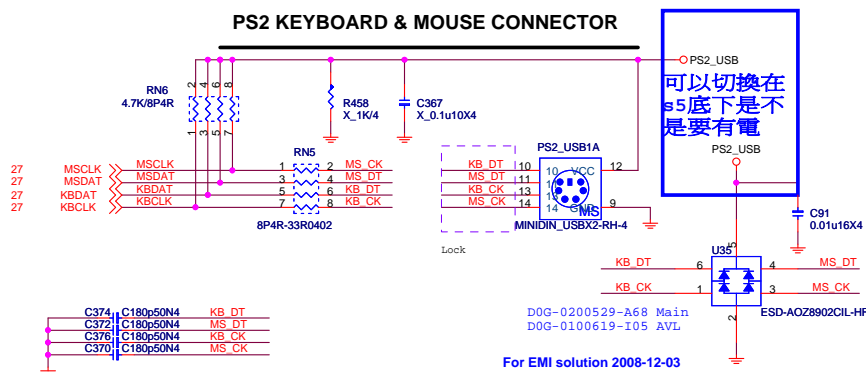
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| Size                           | Document Description        | Rev |
|--------------------------------|-----------------------------|-----|
| Custom                         | Rear I/O & USB2.0 Connector | 10  |
| Date: Thursday, March 20, 2014 | Sheet 26 of 41              |     |

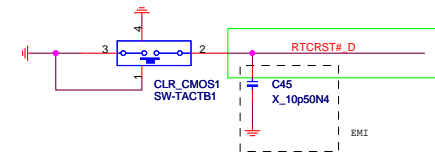


## PS2 KEYBOARD & MOUSE CONNECTOR



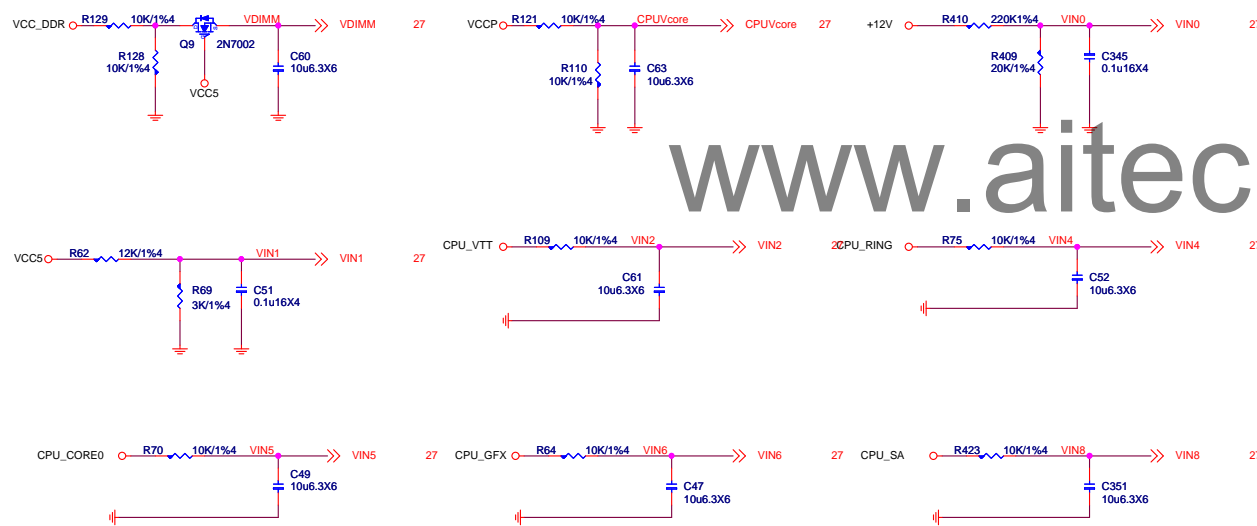
HW MODE

Clear CMOS Button

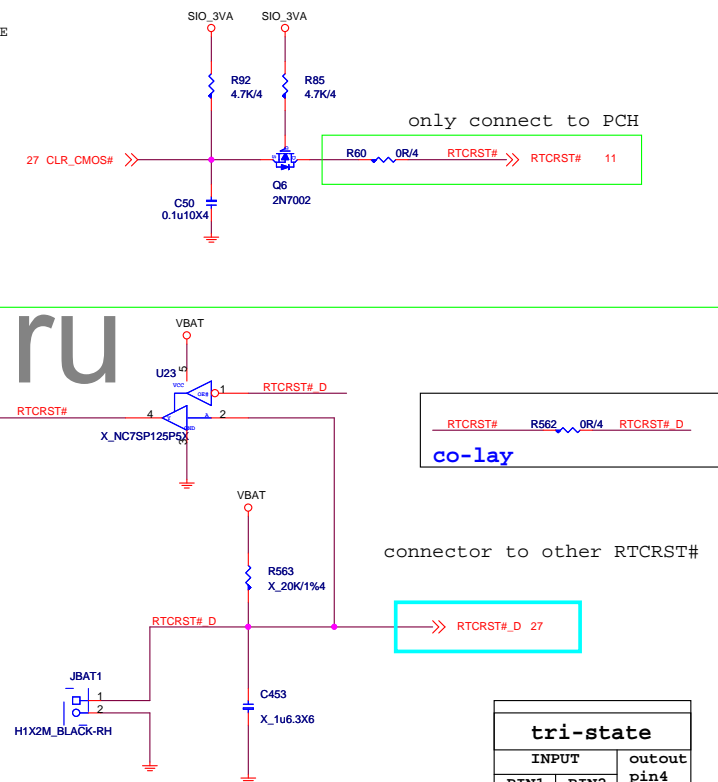


## HW Monitor - Voltage

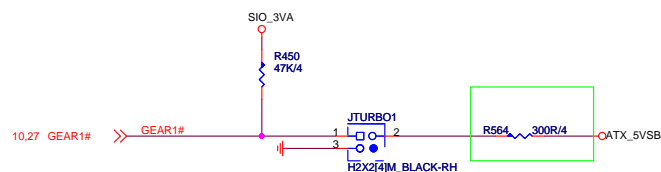
SIO HM Voltage voer 2V will not detect



BIOS MODE



TURBO\_MODE#



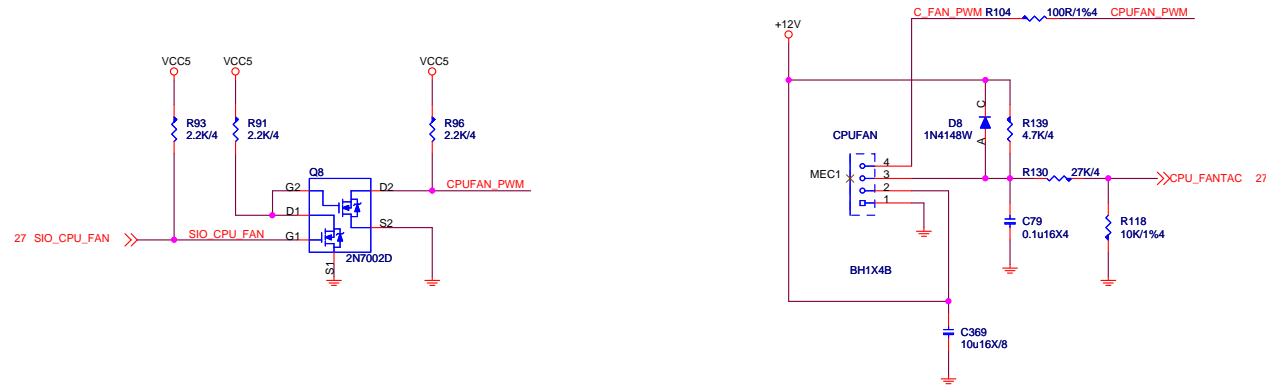
MICRO-STAR INT'L CO.,LTD

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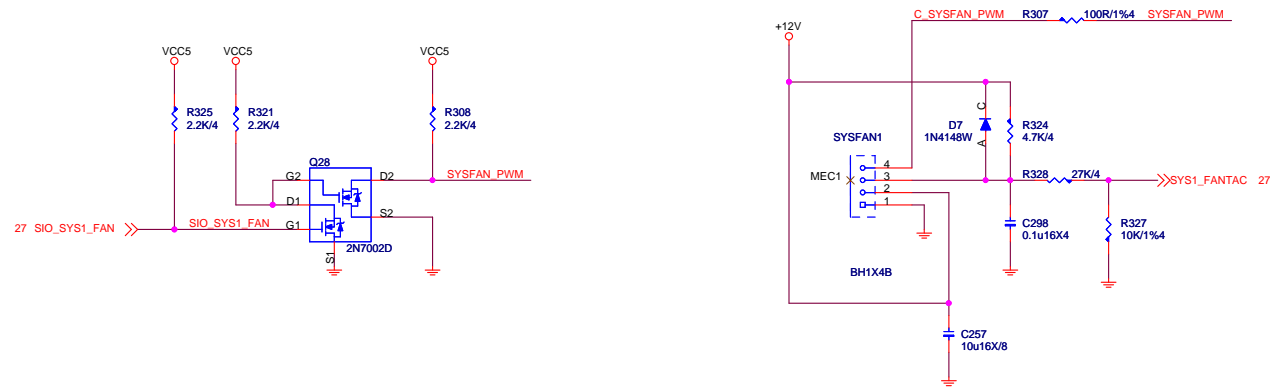
| Size                           | Document Description | Rev |
|--------------------------------|----------------------|-----|
| Custom                         | SIO-NCT6792D/PS2     | 10  |
| Date: Thursday, March 20, 2014 | Sheet 28 of 41       |     |

# FAN-COUNTROL CIRCUIT

CPUFAN TYPE E



SYSTEM FAN1 (PWM MODE)



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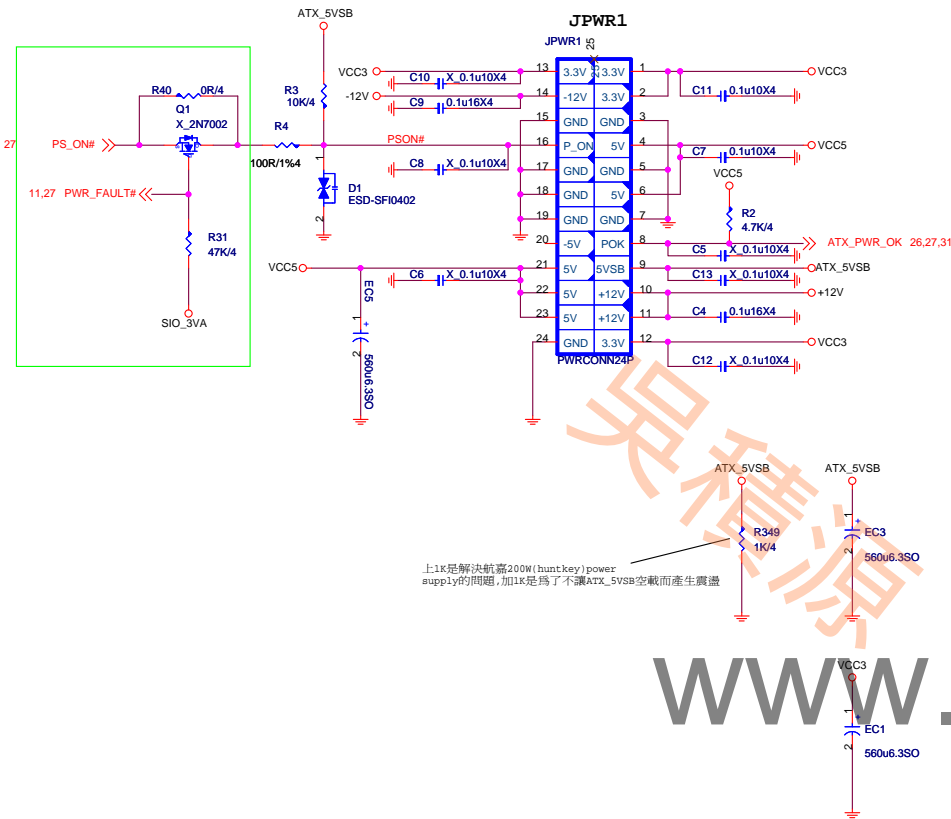
MICRO-STAR INT'L CO.,LTD

MS-7920

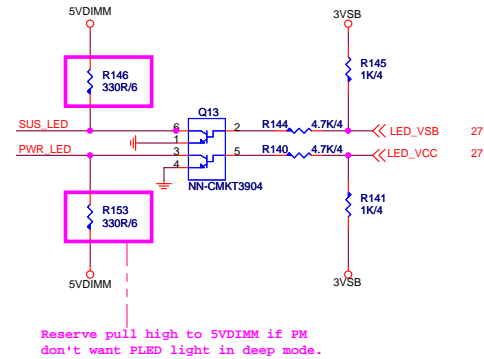
|        |                          |                |
|--------|--------------------------|----------------|
| Size   | Document Description     | Rev            |
| Custom | FAN Control              | 10             |
| Date:  | Thursday, March 20, 2014 | Sheet 29 of 41 |



## ATX POWER CONNECTOR

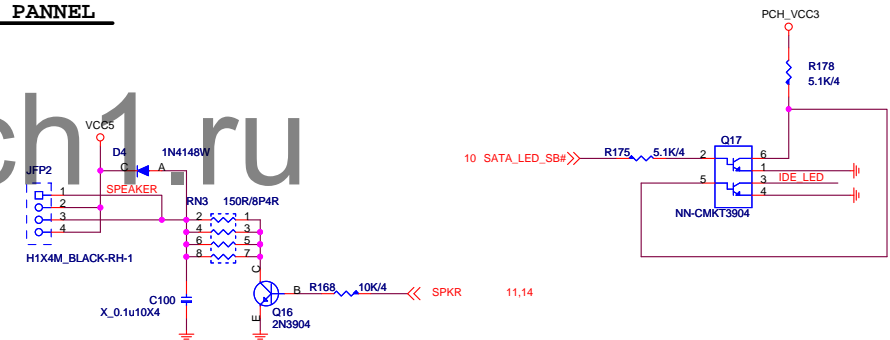


## LED ( for Fintek NTC6779D)

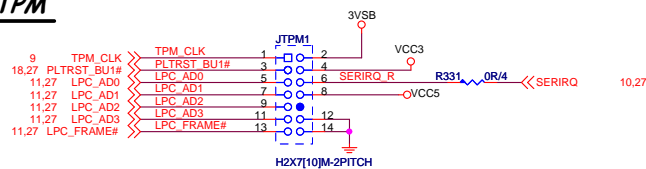


## 5VCC leakage from ATXP6D

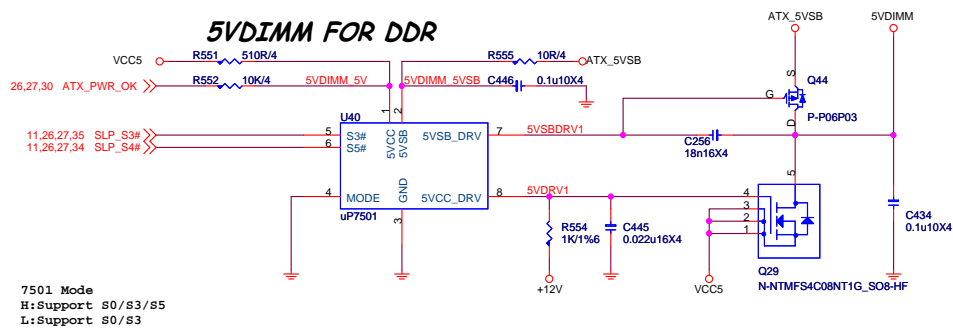
## FRONT PANNEL



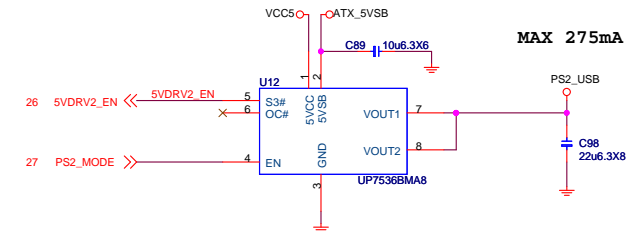
## TPM



## 5VDIMM FOR DDR



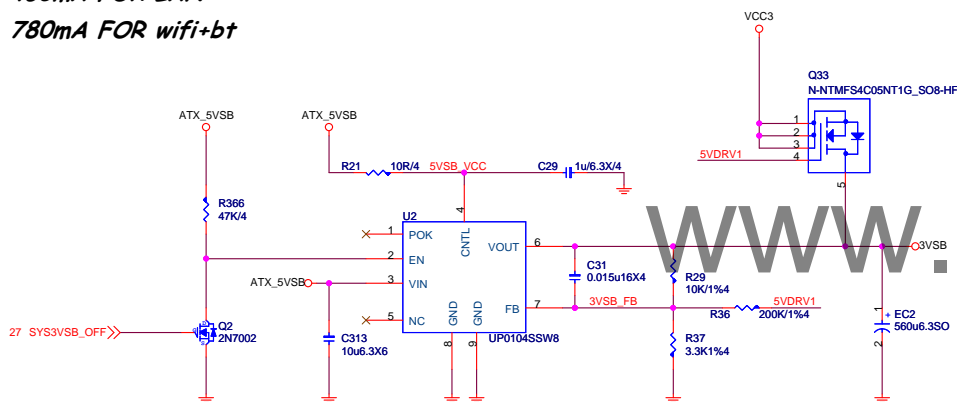
## PS2 Power



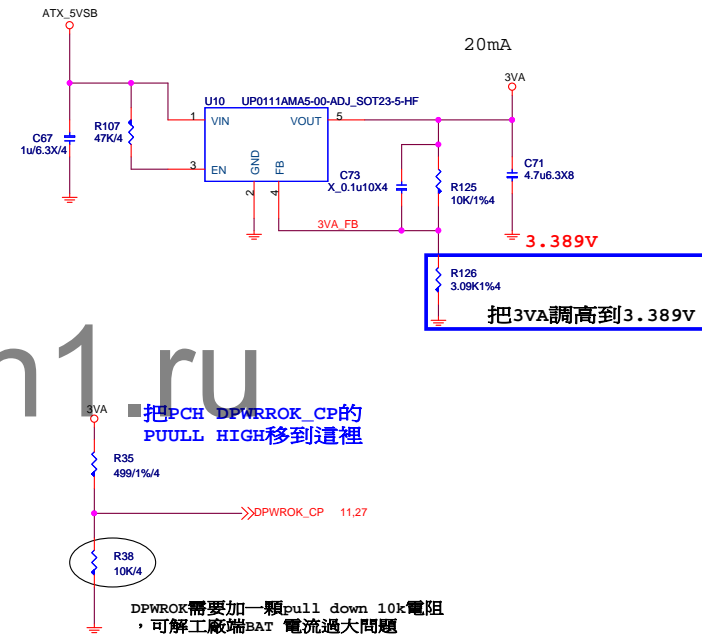
## 3VSB

$$3VSB: 0.216A + 0.375A + 0.46A + 0.78A = 1.831A$$

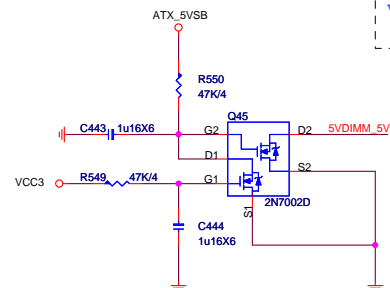
216mA FOR PCH  
375mA FOR PCIE  
460mA FOR LAN  
780mA FOR wifi+bt



## 3VA



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.



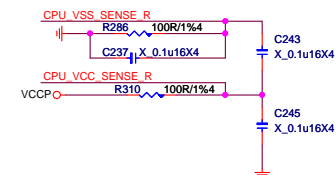
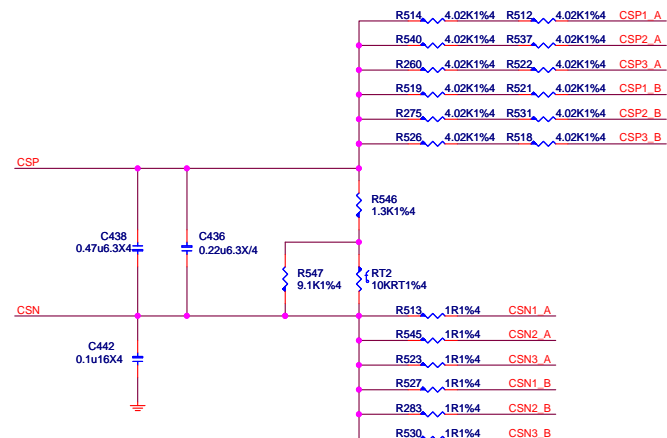
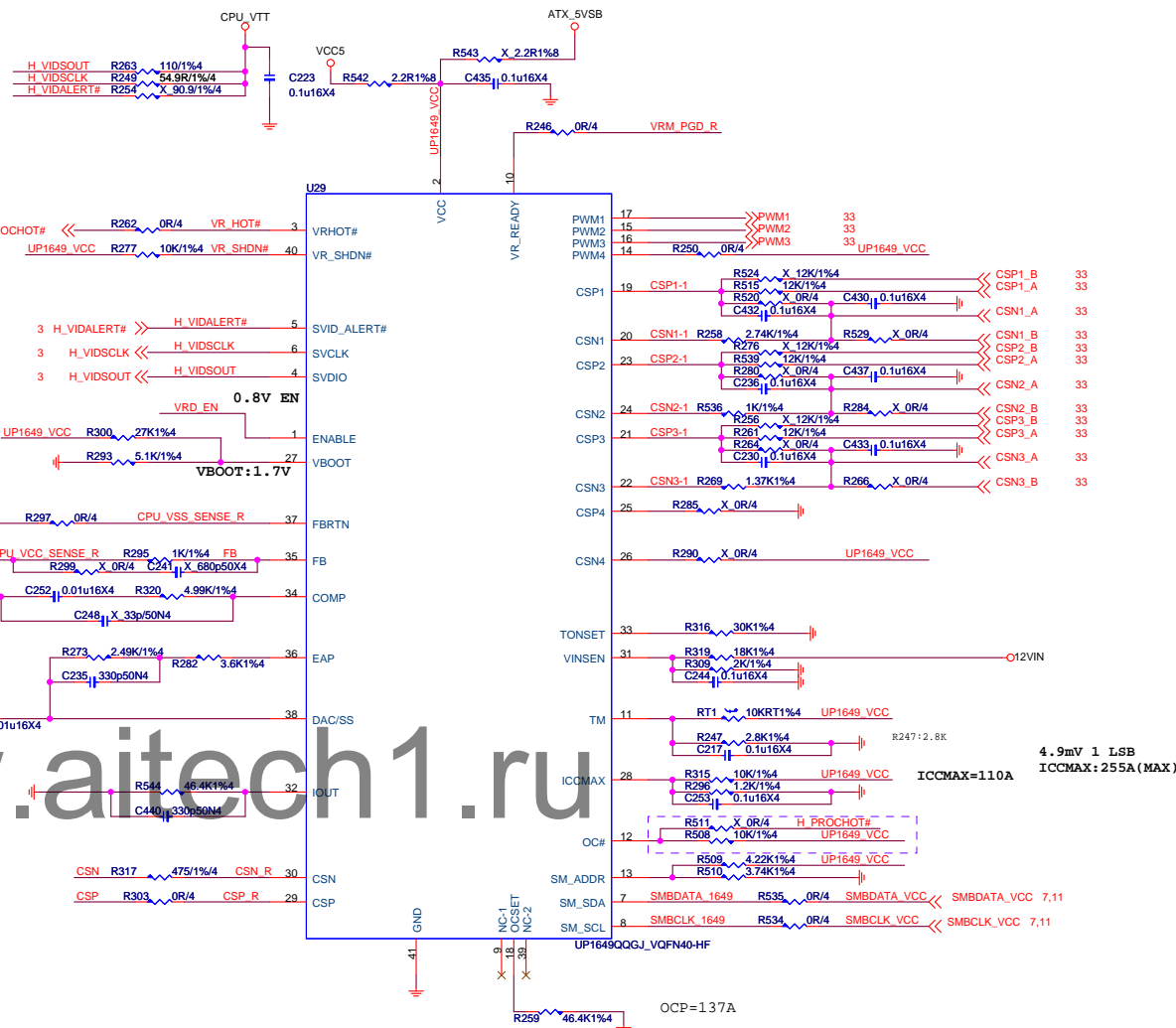
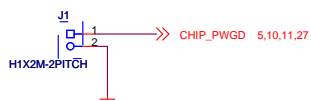
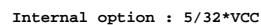
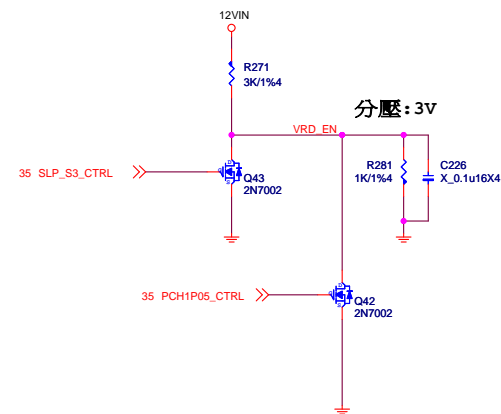
GPIO13 from PCH

TO ALL PCIE SLOT RESET#

Remove AND

PCIE\_SLOT\_RESET\_N  
from SIO RESET\_BUS2

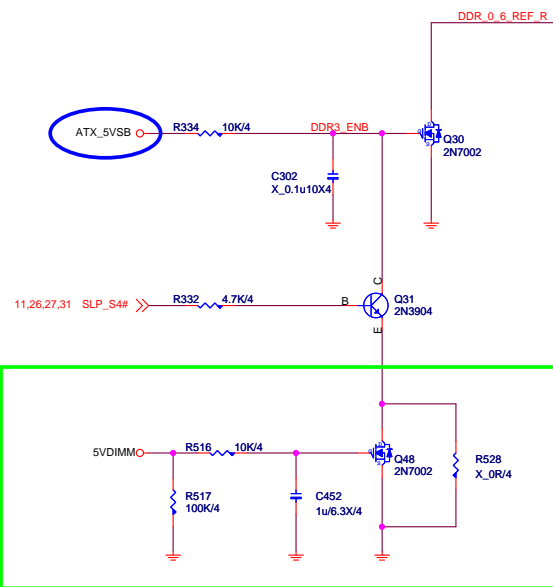
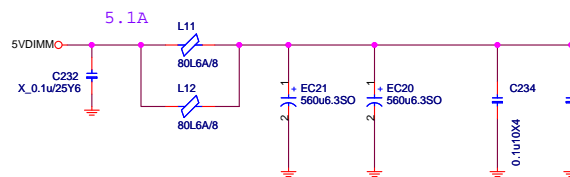
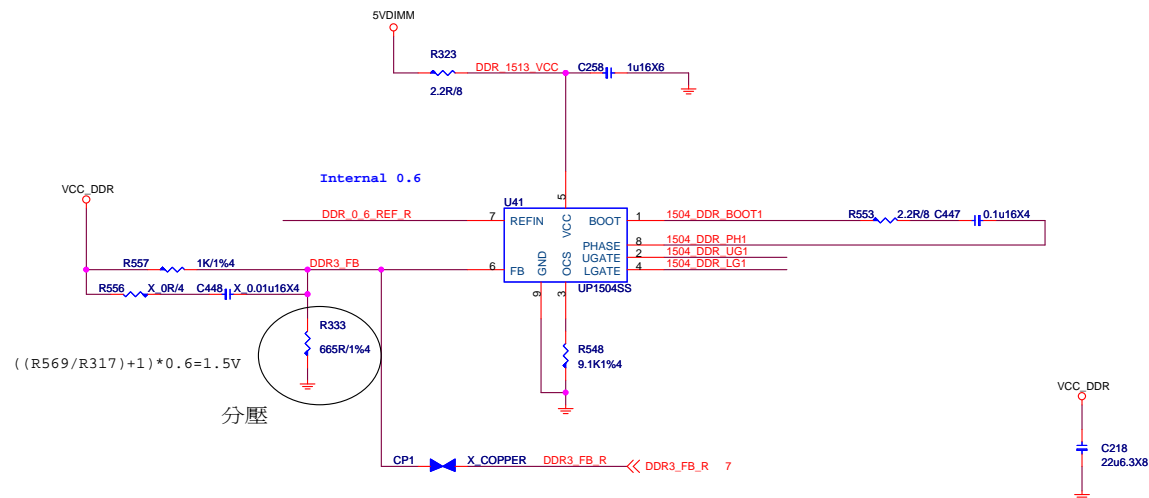
| MICRO-STAR INT'L CO.,LTD |                          |       |          |
|--------------------------|--------------------------|-------|----------|
| MS-7920                  |                          |       |          |
| Size                     | Document Description     | Rev   |          |
| Custom                   | ACPI controller UPI      | 10    |          |
| Date:                    | Thursday, March 20, 2014 | Sheet | 31 of 41 |

**MS-7920**

|                                |                                                 |                |
|--------------------------------|-------------------------------------------------|----------------|
| Size<br>Custom                 | Document Description<br><b>VRM12.5 - UP1649</b> | Rev<br>10      |
| Date: Thursday, March 20, 2014 |                                                 | Sheet 32 of 41 |



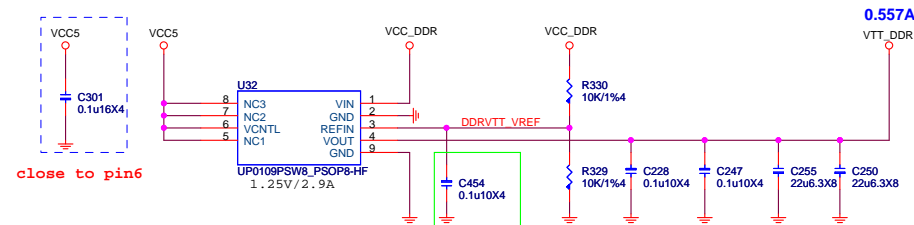
***R320=9K ohm***



P.S. Only for meet Intel power down sequence.



To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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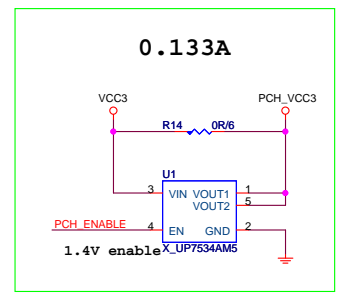
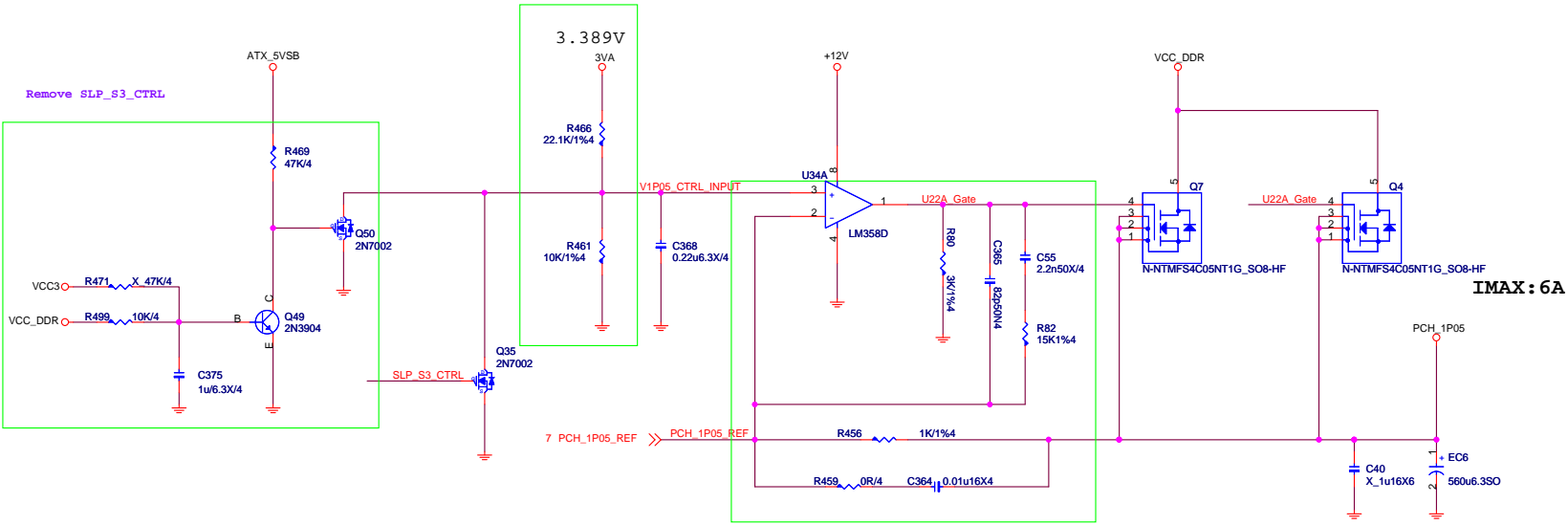
**MS-7920**

|                                |                                                            |                |
|--------------------------------|------------------------------------------------------------|----------------|
| Size<br>Custom                 | Document Description<br><b>DDR POWER - UP1504S -2PHASE</b> | Rev<br>10      |
| Date: Thursday, March 20, 2014 |                                                            | Sheet 34 of 41 |

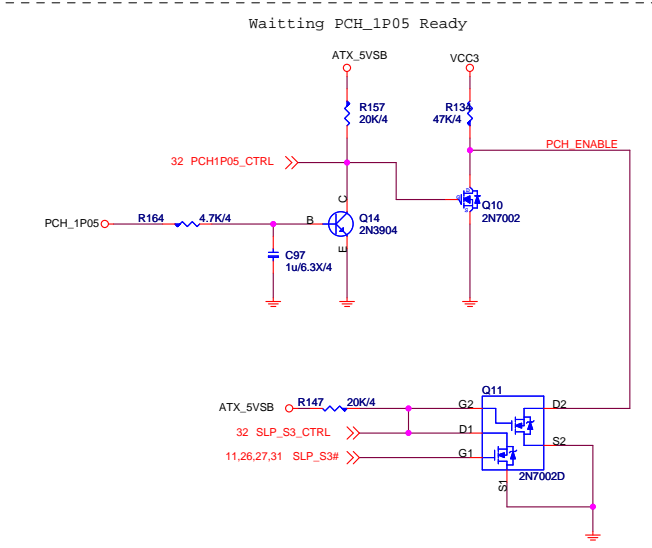
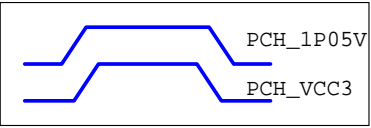
PCH Power:1.05V  
PCH Core 6A

Iripple=1.80A  
5\*1=5A>1.80A  
Iout ripple = 5A

PCH Power:3.3V



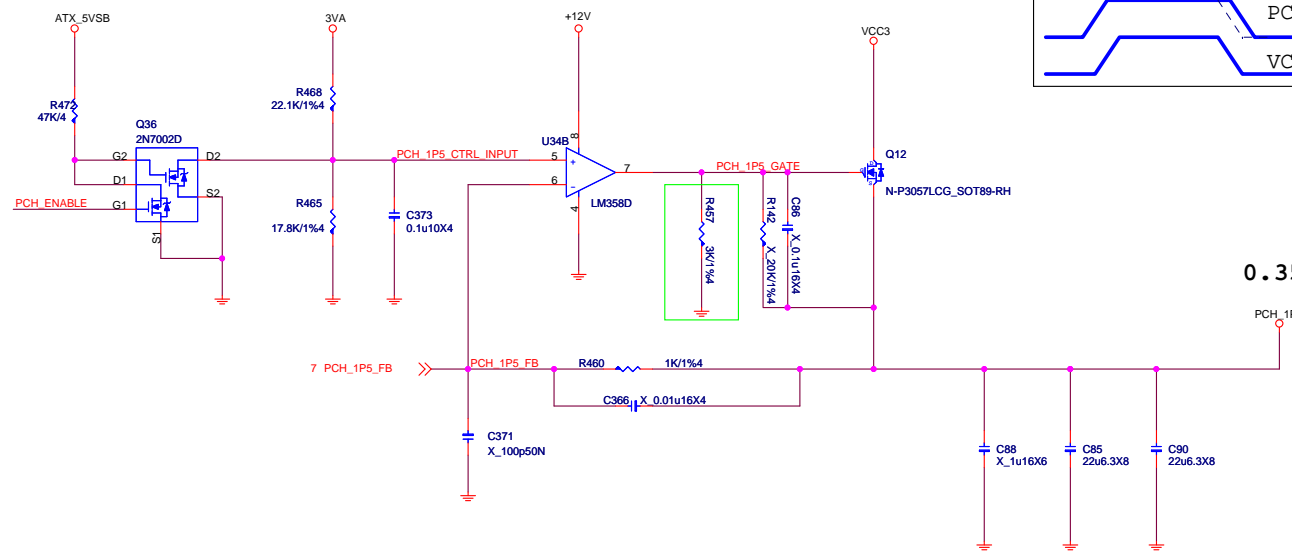
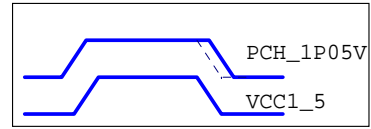
VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH



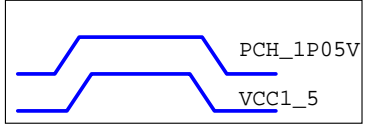
PCH Power:1.5V  
PCH: 0.35A  
PCH\_1P5  
I<sub>max</sub>: 0.35A

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VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH



VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH



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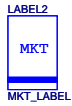
|                                                                                       |                      |       |                          |       |
|---------------------------------------------------------------------------------------|----------------------|-------|--------------------------|-------|
|  |                      |       | MICRO-STAR INT'L CO.,LTD |       |
|                                                                                       |                      |       | MS-7920                  |       |
| Size                                                                                  | Document Description |       |                          | Rev   |
| Custom                                                                                | EMI CAP              |       |                          | 10    |
| Date: Thursday, March 20, 2014                                                        |                      | Sheet | 36                       | of 41 |



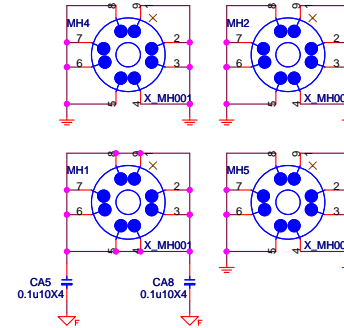


7920\_10

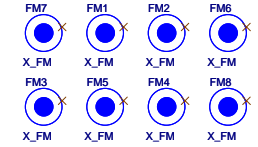
PD0-0792010-G37,精成,23,寶安恩斯邁廠(MSIS)  
PD0-0792010-G37,精成,77,寶安恩斯邁廠(MSIS)  
PD0-0792010-E48,競華,23,寶安恩斯邁廠(MSIS)  
PD0-0792010-E48,競華,77,寶安恩斯邁廠(MSIS)



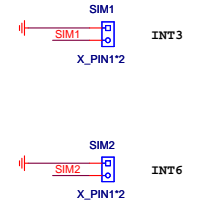
## Mounting Holes



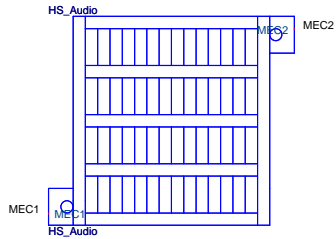
## Optical Fiducial Marks-120



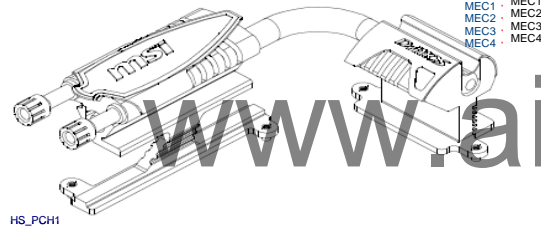
## Simulation



## HEATSINK



HS\_PCH1



MS-7920-0A 主BOM為Z97

| OPT | Configure | BOM          | Function                                                                                                    | BOM GPIO Setting(GP69/GP70/GP71) |
|-----|-----------|--------------|-------------------------------------------------------------------------------------------------------------|----------------------------------|
|     | H87M-G43  | 601-7920-A10 | MS-7920 0A Z97I GAMING AC,Z97,LGA1150,2DDR3,1PCI-Ex16,1mini PCI-E,4SATA3,4USB2,6USB3,HD Audio,GbLAN,HDMI,DP | 0,0,0                            |



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MS-7920

| Size                           | Document Description | Rev |
|--------------------------------|----------------------|-----|
| Custom                         | Manual parts         | 10  |
| Date: Thursday, March 20, 2014 | Sheet 37 of 41       |     |